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DIGITAL BEAM STEERING ANTENNA

General Electric Company

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19 ABSTRACT (Continue on reverse if necessary and identify by block number)

A study and evaluation was made of self-calibration techniques applicable to an elemental receiver, digital beamforming receive array requiring precise pattern control (low sidelobes, adaptive nulling, and large dynamic range). A test bed, C-Band, 32-element line array incorporating a novel loop calibration concept was designed and implemented. The test bed array includes 32 elemental receivers with I and Q digital outputs; the array will be used in experiments evaluating the effectiveness of the self-calibration technique.

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SUMMARY

The objective of this work was to study and evaluate the use of self-calibration techniques and circuitry, for an array with digital beam processing, as a means of achieving precise pattern control (low sidelobes, adaptive nulling and high resolution) over large bandwidths and large dynamic range. Calibration techniques for digital beamforming in the receive mode for radar surveillance applications was emphasized but techniques applicable to the transmit mode and communication applications were also of interest. The work was divided into a study phase to examine the consequences of various approaches followed by a hardware development phase to design and implement a calibration test bed array antenna to demonstrate the feasibility of self-calibration in the receive mode.

The principal tasks accomplished during the study phase were to:

1) Determine the performance constraints imposed by the array and the various components in a Digital Beamforming Receiver (DBR) up to the array beamformer.
2) Evaluate the effectiveness of a self-calibration implementation approach.
3) Evaluate some architectures for a test bed array.
4) Develop the design specifications for a test bed array.

The principal tasks accomplished during the implementation phase included:

1) Detailed design, fabrication and test of a fixed subarray element for a 32 element digital beamforming array.
2) Fabrication and test of a unique "loop type" calibration feed for the 32 element array.
3) Fabrication and test of 32 elemental receivers with A/D converters.
4) Design, fabrication and test of a recording system to enable calibration and detailed pattern measurements of the 32 element test bed array.

5) Implementation of control software to permit calibration of the array and collection of pattern data on an antenna test range.

This work was undertaken to evaluate the implementation issues that determine the effectiveness digital beamforming arrays as a means of achieving precision control of array patterns over the dynamic range of interest in system applications. Digital beamforming conceptually offers the opportunity to obtain improved adaptive pattern nulling, closely spaced multiple beams, array element correction, super resolution and flexibility in radar time and power measurement. Digital beamforming eliminates the constraints on numbers of beams, beam placement and beam quality (phase and amplitude errors in the beamformer and elements) associated with fixed beamformers; at the same time, the hardware (elemental receivers) which must be added to an array to implement digital beamforming increases the sources of phase and amplitude errors which decrease the quality of array patterns. Self-calibration, at the elemental receiver level, provides the opportunity to eliminate not only the errors introduced by the fixed beamformer but also any errors introduced by limitations in the response of the receiver system. That these improvements are indeed achievable in reasonable cost hardware remains to be demonstrated with detailed measurements of test bed hardware which implements the most promising system approach to calibration.

The efforts on this program were limited to selecting a promising approach to implementing a digital beamforming test bed array, after studying the limitations of components on the array performance; and, implementing a 32 element digital beamforming test bed array and data collection system to permit evaluation of the approach. The detailed characterization of the digital beamforming test bed array and evaluation of beam pattern quality is being performed by members of the staff of

the Electromagnetics Development Center of the Rome Air Development Center at Hanscom Air Force Base, whc were the sponsors of this contract.

The calibration feed used in the test bed array is a unique design which utilizes a single coupling hole, on the main transmission line, for each elemental receiver. In a large array, the insertion phase and amplitude differences in the calibration feed system up to the input to each coupler can be cancelled since the non-directional properties of the coupler permit a test signal to be coupled to a receiver from both ends of a feed which effectively includes the entire feed system transfer function in each insertion phase and amplitude measurement that is made. The self-calibration properties of the test bed calibration feed are offset by a higher insertion loss (as compared to a corporate feed system) and higher susceptibility to coherent combining of mismatch error effects. It is potentially possible to introduce path length differences in the construction of the calibration feed to partially decorrelate mismatch error effects and/or measure the feed system and subtract out calibration feed errors. Additional development work is recommended to develop a calibration feed system that yields minimizes calibration feed induced errors into an array calibration.

PREFACE

The development work on the Digital Beam Steering Antenna (DBSA) project was carried out by the Advanced Development Engineering Subsection of General Electric's Radar System Department. The principal contributors and consultants to the work accomplished on the DBSA project include Richard Kinsey (Program Manager), Dr. Gerry Otteni, James Stitts, Richard Taylor, Robert Jackson, Ruth Brown, Charles Vernon and Sidney Applebaum.

The DBSA contract was sponsored by the Electromagnetics Development Directorate of the Rome Air Development Center (RADC) at Hanscom Air Force Base, Ma. The RADC project technical contract manager was Nicholas P. Kernweis with Dr. Hans Steyskal as the alternate manager. The data for interfacing into the RADC antenna pattern measuring equipment was provided by Jeffrey Herd.

The following contracts cover work related to the DBSA project:

1) Digital Beamforming Receiver Modules, U.S. Army Missile Command, Redstone Arsenal, Al, DAAH 01-86-C-0177.

2) Mainbeam ECCM Definition/Implementation/Experimentation, Rome Air Development Center, Griffiss AFB, N.Y., F30602-86-C-0260.

C Band Receivers, Base Contracting Division, 416 BMW/LGC, Griffiss AFB, N.Y., F30635-85-C-0120

4) Digital Beamforming Radar (DBR) Study, U.S. Army Missile Command, Redstone Arsenal, Al, DAAH 01-83-C-A119.

5) Anti-Arm Radar Techniques Development, Harry Diamond Laboratory, DAA21-80-C-0131.

6) Signal Processing Requirements for Digital Beamforming, System Development Corp., 76-427, DASG60-76-0027.

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SECTION 1
INTRODUCTION

In the Digital Beam Steering Antenna (DBSA) project, the effectiveness of self-calibration techniques was studied as a means of minimizing the system limitations of the antenna array and elemental receiver components in achieving precise control of array patterns. Performance bounds of a Digital Beam Forming (DBF) array were established based on the expected performance of the individual array components; the impact of self-calibration as a means of compensating for relaxed component requirements was investigated.

DBF conceptually offers the opportunity to obtain precise control of the array transfer function starting at the individual array elements. This can provide the flexibility needed in beam pattern control to achieve:

1) Improved adaptive pattern nulling and the ability to place multiple nulls in a pattern in response to the external ECM environment.
2) Closely spaced multiple beams to increase data rates and the dwell time in a beam position as a means of countering high speed, low radar cross section target threats.
3) Super resolution to permit multiple targets to be resolved and accurately tracked to discriminate between close spaced decoys and threats.

DBF provides operational flexibility which is either not practical or not possible in RF beam formers. In a digital beam former each beam can be uniquely weighted to achieve specific sidelobe objectives or resolution; beams can be closely spaced, clustered in groups or variably spaced to meet any spatial and energy management set of criteria. At the same time, however, the elemental receiver circuitry (and local oscillator distribution circuitry) which must be added to an array to implement DBF increases the potential sources of phase and amplitude errors. The additional error sources must be bounded and compensated for in order to not degrade the quality

of the array patterns below what can be achieved from an optimized r-f beam former.

Self-calibration, at the elemental receiver level, provides the opportunity to correct insertion phase and gain errors from the calibration reference point up to the A/D converter output. In principal, all errors introduced by limitations in the insertion gain and phase response of the receiver system can be compensated for (except inadequate dynamic range). The viability of the calibration process to compensate for errors is credible when the insertion gain and phase errors are essentially constant over the instantaneous signal bandwidth and can be treated as fixed bias errors at the operating frequency. Detailed measurements of a test bed hardware implementation of a system approach to calibration is required, however, to verify that high performance digital beam forming can be achieved with reasonable cost hardware.

The work on this project was divided into a study phase and an implementation phase. The study phase addressed the use of self-calibration techniques and circuitry as a means of achieving precise pattern control (low sidelobes, adaptive nulling and high resolution) over large bandwidths and large dynamic range in an array with provisions for digitally forming beams. The study was primarily directed towards calibration techniques which would be applied to the receive mode in radar surveillance applications. The calibration approaches that were examined were also applicable to communications arrays and determining the phase and amplitude error corrections needed at the element level for the transmit mode. The sources of errors and types of errors seen in a digital beam forming array were studied and the consequences of applying various approaches to measuring and correcting such errors were evaluated.

In the implementation phase, a digital beam forming line array test bed was built to be used as a test vehicle to evaluate digital beam forming array performance. The test bed includes 32 receive elements, a self-calibration system, 32 elemental receivers, an exciter, a data recording interface to the HP9836 desk top computer and the software to calibrate the

array, form beams and generate beam pattern responses for any beam position.

The array testing was limited to detailed measurements of the individual assemblies and a validation of the operation of the overall array in the calibration mode and data recording mode. The array tests were made with the array fixed in position and pointed directly at a far field source.

The detailed characterization of the digital beam forming test bed array and evaluation of beam pattern quality is being performed by members of the staff of the Electromagnetics Development Directorate of the Rome Air Development Center at Hanscom Air Force Base, who were the sponsors of this contract.

SECTION 2

DBSA STUDY PHASE

2.1 INTRODUCTION

The tasks performed during the study phase included:

1) Determination of the performance constraints on digital beam forming imposed by the array and receiver components.
2) Evaluation of the effectiveness of an implementation approach for a calibration system concept.
3) Evaluation of architectures for a test bed array.
4) Preparation of specifications for a test bed array.

The principal sources of errors in the array system components were analyzed to evaluate the impact of the component specifications on the quality of digitally formed beams. Test data was obtained on the SAW filter and the A/D converter, two receiver components which have the most impact on the digital beam forming. A SAW filter is used to control the receiver signal bandwidth to reduce variations in phase and amplitude responses between receiver channels; the response match that can be achieved between SAW filters is then a critical receiver design factor. The dynamic range, linearity, phase and amplitude response of the A/D converter all have an impact on the quality of digitally formed beams; the match between receiver channels and the overall response of the receiver channel is, therefore, largely determined by the performance of the A/D converter.

Insertion phase and amplitude measurements were made on a prototype of a loop type array calibrator to determine the magnitude and correlation of the insertion phase and amplitude errors due to the loop approach and the construction tolerances. The array factor response was computed using the measured errors as the transfer function of the elements.

The study results provided a background for defining the specification for the test bed array that was implemented in the second phase of the contract.

2.2 SYSTEM PERFORMANCE REQUIREMENTS

Performance characteristics of potential tactical planar array surveillance systems are shown in Table 1. Standoff jammer type Electronic Counter Measure (ECM) threats require average sidelobe levels of -55 dB and peak sidelobe levels less -50 dB, over critical sectors in the scan coverage. Self screening jamming threats require adaptive cancellation techniques and a large receiver dynamic range (70 dB) to offset high jamming levels.

Signal bandwidth requirements range from 0.5 to 200 MHz. Long range surveillance requirements can be satisfied with signal bandwidths as low as 0.5 MHz; most track applications can be satisfied with bandwidths of 5 to 20 MHz. Bandwidths higher than 20 MHz may be needed to track targets in dense raids or to evaluate miss distances during intercepts; wide bandwidth, however, is usually only required over a limited range window. The widest signal bandwidth requirement is target identification where high range resolution is needed to obtain sufficient detail in the target signature; 200 MHz is the lower bound on bandwidths that would have any value in this application.

If only a limited range windows is required for the high bandwidth applications, a Linear Frequency Modulated (LFM) signal can be transmitted and deramped to CW on receive. The deramping occurs at an early point in the receive chain to minimize the hardware which must have high bandwidth. The reduction in bandwidth is particularly important in a digital beamforming array since it allows the A/D converters and digital beamformer parameters to remain unchanged from that used for the low bandwidth all range waveforms. The response of all of the circuits which precede the output of the deramping mixer, however, must be phase and amplitude matched over the high bandwidth signal to achieve low sidelobes as in the case of conventional arrays. Time delay compensation may also be required across the array for high signal bandwidths to attain low range sidelobes for off broadside targets.

TABLE 1. Potential requirements for a surveillance radar

Parameter	Value
Array Gain	38 - 41 dB
Number of elements	2000 - 4000
Average sidelobe levels	< -55 dB
Peak sidelobe levels	< -50 dB
Azimuth coverage	± 45° minimum
Elevation coverage	0 to 30° minimum
Dynamic range	70 dB minimum
Signal bandwidth	0.5 - 200 MHz

The characteristics of an example 4096 element array with 5 dB gain elements are shown in Table 2. To achieve -50 dB peak sidelobe levels with typical uncompensated errors, a -55 dB Taylor weighting taper has been assumed in both planes for sidelobe level control. The array directive gain, after weighting is 37.6 dB. To achieve -50 dB peak sidelobes, the rms sidelobes must be about -58 dB or -20.4 dB below isotropic gain. Only small correlated errors, at the row or column level of the array, can be tolerated in the array and achieve the desired sidelobe levels.

TABLE 2. Example planar array parameters

Parameter	Value
Array peak sidelobe level	- 50 dB
Array rms sidelobe level	- 58 dB
Number of elements	4096
Taylor weighting level (each plane)	- 55 dB
Element gain	5 dB
Elemental phase errors	
Row or column correlated (max.)	0.33° rms
Uncorrelated (max.)	2.2° rms
Elemental gain errors	
Row or column correlated (max.)	0.05 dB rms
Uncorrelated (max.)	0.32 dB rms

The composite of the errors from all the components which comprise the elemental signal path must be controlled to the level shown in Table 2 for -50 dB peak sidelobes. The elemental signal path includes a radiating element, an elemental receiver (r-f input to A/D converter output), an LO distribution system and all interconnecting signal cables in the digital beamforming array. It would be impractical to build a digital beamforming array with the channel matching (after alignment) specified in Table 2 to operate over the environmental range if periodic corrections of the insertion phase and gain could not be made. An on-line calibration system is required to measure the elemental signal paths for component drift with temperature, operating voltage and time (component aging) in order to compensate the array. A comprehensive calibration system can reduce performance requirements on individual components and thereby reduce the fabrication cost of the array. Ideally the calibration system should include all of the elemental signal path components to allow the widest tolerance in the elemental signal path components. The calibration system itself must include provisions to compensate for insertion phase and gain errors within its signal paths and have a residual error significantly less then the error bounds shown in Table 2.

2.3 ELEMENTAL RECEIVER ARCHITECTURES AND IMPLEMENTATIONS

The digital beamforming array is characterized by (and limited by) the capabilities of the elemental receivers used in the array. The generic digital beamforming receiver contains the following functional elements:

1) A low noise amplifier to establish system noise figure.
2) A preselection filter to eliminate image band interference from the receiver.
3) One or more stages of down conversion to translate the receive signal to a suitable frequency band for signal spectrum match filtering and A/D quantization.
4) A filter to limit the spectrum width of the signals that are quantized.

5) A quantizer (A/D converter) subsystem.
6) Signal level overload control circuits.
7) Insertion phase and gain correction provisions.
8) Monitoring circuitry.

Since the elemental receivers are a significant factor in the cost of a digital beamforming array; it is important to use an architecture which is low cost and yet meets performance requirements. Channel to channel response match and dynamic range are the most critical performance factors of the elemental receiver since they determine the wide band noise interference adaptive cancellation performance of the digital beamforming array. Potential elemental receiver architectures and their relative capabilities are considered in the discussion which follows.

2.3.1 Single down conversion receiver. The single down conversion receiver (Figure 1-a) has the simplest architecture and is potentially low in cost. A bandpass filter is required prior to the down conversion mixer to eliminate out of band interference. The highest dynamic range is attained when the filter precedes the low noise amplifier (LNA) to limit out of band interference; the bandpass filter loss, however, then reduces the receiver sensitivity. The synchronous detector LO and the agile LO are merged into one LO, only the synchronous detector mixers are present in the single down conversion receiver.

The simplicity of the architecture of the single down conversion receiver is offset by significant deficiencies in its performance. When the synchronous detector LO frequency is changed, to tune the receiver over the operating band, the synchronous detector DC levels and in-phase and quadrature components balance may be expected to change. The synchronous detector outputs require compensation at each operating frequency because of phase and amplitude changes in the mixers as a function of LO frequency.

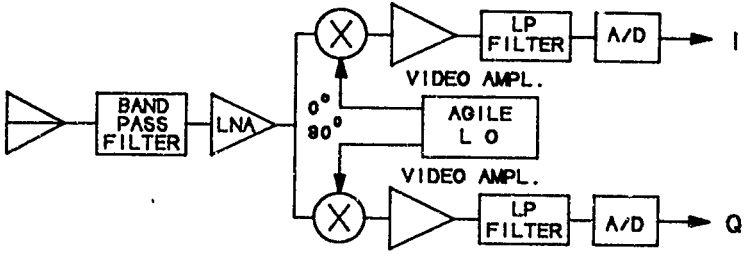

Figure 1a. Single-Conversion Elemental Receiver

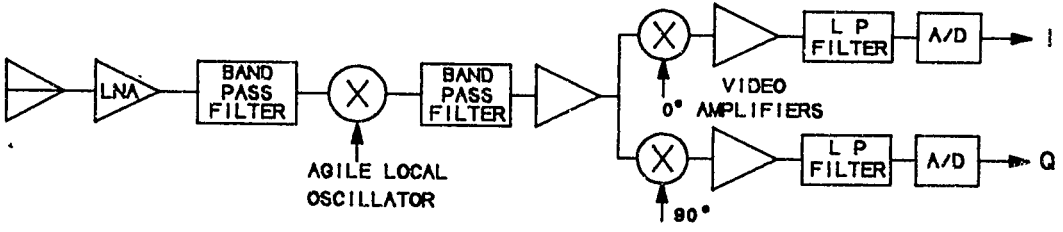

Figure 1b. Double-Conversion Elemental Receiver

The phase and amplitude relationship (over the signal bandwidth) between the in-phase (I) and quadrature-phase (Q) outputs of the synchronous detector is also determined by the match between the two low pass filters following the synchronous detectors. The low pass filters normally determine the signal bandwidth; stringent phase and amplitude matching requirements across the signal bandwidth make the filters difficult to build and hence expensive.

With only two amplifiers in a single down conversion receive, it is difficult to realize large dynamic range, low noise figure and stable transfer characteristics. The C-band low noise amplifier (LNA) and video amplifiers must have sufficient gain to offset all receive losses and raise the receiver self noise level to the quantization level of the A/D converters. There are adverse factors with having large gain in either the LNA and video amplifiers. The dynamic range available from the synchronous detectors limit how much gain can be placed in the LNA before receiver dynamic range is impacted. Having high gain in the video amplifier leads to larger variations the DC unbalance of the receiver. The noise figure of high output video amplifiers is usually poor, it is therefore undesirable to have large gain in the video amplifier to avoid increasing the receiver noise figure.

The previous deficiencies in the single down conversion receiver make it unsuitable for high performance digital beamforming despite its low implementation cost.

2.3.2 Double conversion receiver. The double conversion receiver shown in Figure 1b has a fixed LO for the synchronous detector reference; the synchronous detector balance and compensation is therefore independent of the agile operating frequency. The first bandpass filter in the receiver, as in the preceding receiver, is required in order to reject out of band interference at the image response frequencies of the agile mixers.

The agile mixer i-f output frequency must be high enough that the image frequencies of the agile mixer can be rejected by

the C-band image rejection filter. A 10% agile bandwidth requires an i-f frequency of approximately 1 GHz. A bandpass filter matched to the signal spectrum can not be used at 1 GHz because of the poor filter to filter match when the ratio of the bandpass to the center frequency of the filter is small. Low pass filters are, therefore, still required to set the signal bandwidth of the double conversion receiver. Although the match between receiver channels is improved by going to a double conversion receiver there is still significant difficulty in attaining the channel matching needed for very low sidelobes. The synchronous detector still operates at a high frequency, which makes the I and Q match more sensitive to the LO distribution variations.

Adding an i-f amplifier, in the double conversion receiver, does allow more flexibility in distributing gain in the receiver. The three amplifiers in the receiver can be configured to have both large dynamic range and low noise figure in the overall receiver.

2.3.3 Triple conversion receiver. The addition of another mixer to the previous receiver architecture gives the triple conversion receiver shown in Figure 2; this architecture allows the frequencies of the i-f stages to be optimized for specific functions. The second i-f frequency can be made low enough to use a bandpass filter, like a surface acoustic wave (SAW) filter, to define the signal bandwidth. The SAW filter, being a finite impulse response filter, has very low phase and amplitude distortion. SAW filters can be built to be closely matched yielding elemental receiver responses which are highly correlated. The lower operating frequency for the synchronous detector makes the detector less sensitive to variations in the LO distribution. The minimum synchronous detector operating frequency is determined by the signal bandwidth and the low pass filtering available to reject the leakage from the LO and r-f inputs to the DC output of the synchronous detector mixers. The triple conversion frequency receiver low pass filters are only used to reduce leakage components from the preceding mixer; they

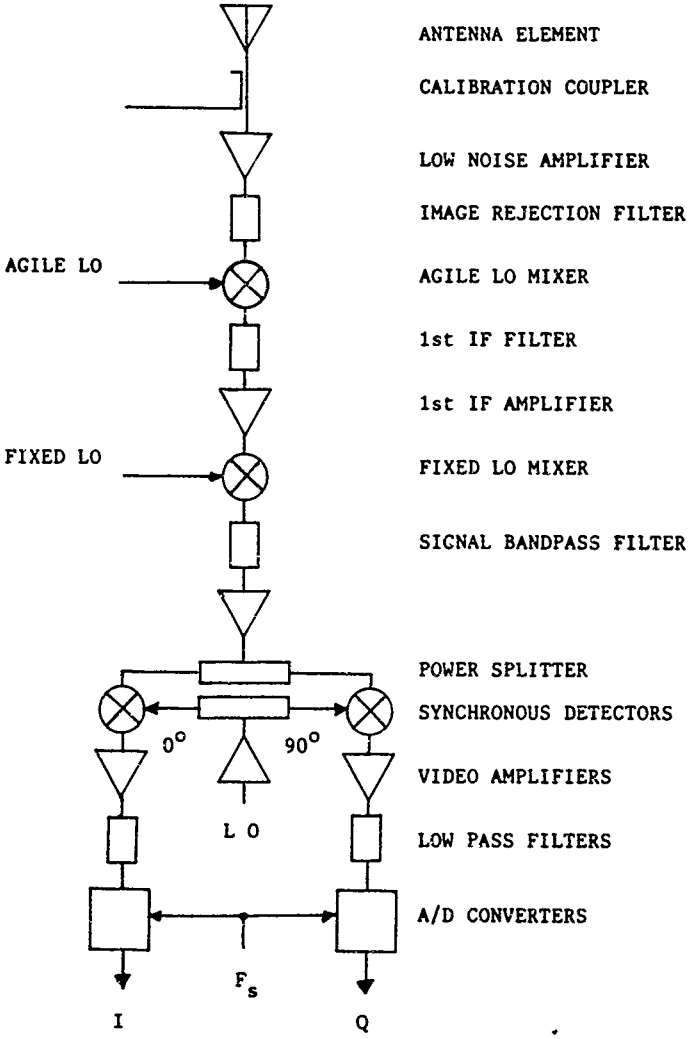

Figure 2. Triple Conversion Receiver

are made much wider then the signal bandpass to assure that they have virtually no impact on receiver matching.

The choice of filter bandwidths and center frequencies for the i-f stages are interrelated and require that compromises be made. The agile bandwidth is a major factor in determining the parameters of the i-f stages. The selection of the i-f filter frequencies is based on image response rejection requirements and the cost of matching responses. As a specific example design, assume a triple conversion receiver designed for a signal band of 5.25 to 5.85 GHz. With an agile bandwidth of 10% of the carrier frequency, the first i-f frequency should be no less than 20% of the carrier (1 GHz) to have practical parameters for an image rejection filter. A 1 GHz first i-f with a low side LO will have image responses from 3.25 to 3.85 GHz from the first down conversion over the agile bandwidth. The first band pass filter cut off rate must be fast enough to attenuate the agile mixer image responses below the interference level (50 dB minimum). High cut-off rates may be achieved with more poles in a filter; however, only a few poles can be used in the filter before variations in the in-band phase and amplitude response between receiver channels affects the cancellation of wide band noise.

A higher first i-f makes the first bandpass filter easier to realize but increases the difficulty of realizing the second band pass image rejection filter. The second pass filter is required to be narrow enough to reject noise interference at the image response frequencies of the third i-f. The third i-f frequently has to be made higher then minimum for the synchronous detector function to make the band pass filter responses more realizable.

The triple conversion receiver has sufficient flexibility to be configured to have large dynamic range, low noise figure and relatively stable transfer characteristics; it is therefore the preferred implementation form for the demonstration equipment.

2.3.4 Base band receiver deficiencies. The last analog operation in the previous receiver architectures was a coherent synchronous detector. The detector yields base band in-phase (I) and a quadrature phase (Q) output signals from mixing the last i-f signal with a reference Local Oscillator (LO). The final signal bandwidth in the receiver is set by the last i-f band pass filter or alternatively by the low pass filters on the I/Q base band signals. The preceding receiver architectures can provide high dynamic range and high rejection of image responses. A major performance limitation in these receivers is the quality of the signal match which can be achieved in the I and Q signals, within a receiver channel and between receiver channels, over the signal bandwidth. The detector quality is determined by the match between the I and Q amplitudes and the degree to which phase quadrature is maintained between the components. Other sources of error includes dc offsets and spurious responses from device non-linearities.

The I and Q match within the channel and between channels is improved when an i-f filter can be used in place of I and Q low pass filters to set the final signal bandwidth. In addition, the i-f filter is lower in cost than a pair of matched low pass filters and smaller in size. However, the synchronous detector, the I and Q video amplifiers and the A/D converters all still potential sources or errors that produce mismatched I and Q signal components and I and Q dc offsets.

DC offset errors can be reduced by DC feed back correction loops (or post A/D conversion bias corrections) when the I and Q DC offsets change slowly over time and have low sensitivity to changes in the ambient temperature and operating voltages.

I/Q mismatch errors in a channel and between channels which are independent of the signal frequency are biases which can be reduced by periodic calibration of the receiver insertion phase and gain at each operating frequency. The final quality that can be achieved in the balance of the I/Q components in a channel and between channels, after compensating for the errors determined from calibration measurements, is limited by the calibration measurement error and the degree to which the I/Q

components were unbalanced prior to compensation. Most of the I/Q component balance errors across the signal bandpass are due to response characteristics differences between the individual I and Q A/D converter and track/hold circuits. It is difficult to obtain A/D converters and track/hold devices which have matched responses across the signal bandwidth and over the signal dynamic range.

2.3.5 Bandpass sampling direct conversion receiver. The base band receiver deficiencies cited in the preceding paragraph can be partially avoided in the bandpass direct conversion type receiver where the signal is quantized while still on an i-f carrier. In the direct i-f sampling receiver architecture, illustrated in Figure 3, only a single A/D converter is used to take real samples of the i-f signal; a digital bandpass filter is used to select the signal spectrum. The input to the digital filter is real samples and the output is base band I and Q pairs. The A/D converter sampling rate for the direct conversion receiver must be at least twice that of the base band I/Q receiver pair of A/D converters since only real samples of the i-f signal are taken. In practice, because of finite cut-off rates in the analog filter and in the signal spectrum, the A/D sampling rate must be made several times higher to reduce mismatch errors from folded over signal spectrum errors. In a typical application, the sampling rate of the single converter will be five times higher then that used for the base band converters for the same signal bandwidth.

Since the I and Q outputs are formed in a digital filter in the direct i-f conversion receiver, I and Q matching problem are effectively eliminated from the channel. The sampling jitter requirements of the quantizer in the direct i-f carrier sampling architecture, are higher then in base band receiver, however, because the carrier frequency must be accurately sampled to recover the signal phase information.

The complexity of the receiver (measured by number of components eliminated) can be significantly reduced in a direct i-f conversion receiver if the i-f sampler is placed at the

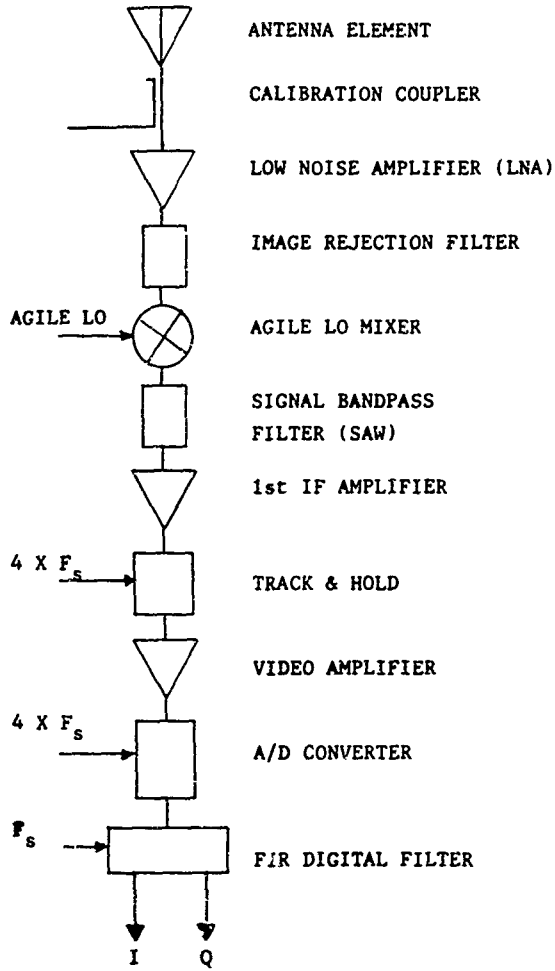

Figure 3. Bandpass Sampling Direct Conversion Receiver

highest i-f frequency that can be sampled and still meet dynamic range and matching requirements. The i-f frequency choice is bounded by the aperture size and jitter of the track and hold (T/H) amplifier since this determines the error in quantizing the i-f signal. Although the T/H aperture size and jitter must be low enough to accurately sample the i-f carrier, the sampling rate will still be low since it is determined by the bandwidth of the signal modulation. Since the T/H amplifier samples are spaced many i-f cycles apart, the i-f frequency will be highly under sampled and there is significant aliasing of the signal. With the proper choice of i-f frequency, signal bandwidth and sampling rate, the aliased portion of the signal spectrum can be positioned to fall into the rejection region of the digital filter. A band pass filter approximately matched to the width of the signal spectrum must precede the T/H amplifier, however, to limit the bandwidth of the noise and exclude out of band interference that would be aliased into the output pass band.

The sampling requirements of the preceding high i-f direct i-f sampling receiver are illustrated by the following specific case. In a C-band receiver with a 2.0 MHz signal bandwidth, a 10 MHz sampling rate can be used with an i-f carrier of 697.5 MHz to sample the signal and alias the results onto a 2.5 MHz carrier. There will also be an aliased frequency response at 7.5 MHz (or equivalently -2.5 MHz), which will be rejected by the digital filtering following the A/D converter. The T/H sampling aperture jitter must be less then 0.45 picoseconds to limit the maximum sampling error to 0.5 of the lsb on an 8 bit A/D converter at the 697.5 MHz carrier frequency.

The limitations in sampling aperture for currently available T/H amplifiers make it impractical to build a direct i-f bandpass sampling receiver operating at a 697.5 MHz i-f. In addition, the current technology for SAW bandpass filters at 697.5 MHz does not provide transition rates between the pass band and rejection region which are adequate enough to limit folding of undesired spectrum into the pass band. Further, SAW filter material reproducibility and etching tolerances are

insufficient, at 697.5 MHz, to obtain filter responses which match well enough for -50 dB peak sidelobes.

2.3.6 Direct i-f receiver conversion alternatives. Although the T/H amplifiers and sampling apertures in current A/D converters are not adequate to build the receiver described in the preceding paragraph. There are advantages in using the direct i-f conversion receiver with an i-f frequency which is near DC but has no significant spectral fold over at DC. This then permits a digital filter to be used to match filter the signal spectrum and produce exact I and Q samples of the signal and eliminates the synchronous detectors.

The receiver architecture up to the final i-f stage is identical between the triple conversion receiver previously discussed and the direct i-f sampling receiver. At the final i-f stage of the direct i-f conversion receiver, the signal is demodulated to a very low frequency i-f carrier. Using the preceding receiver example (paragraph 2.3.5), with a 2.0 MHz signal bandwidth, the final i-f would be at 2.5 MHz and a 10 MHz sampling rate would be required to keep the image response at -2.5 MHz isolated from the desired response. As in the preceding case, a digital filter is used to match the signal spectrum and provide I and Q outputs.

The sampling aperture jitter requirements for the preceding example are reduced to 125 picoseconds for an 8 bit converter and 7.8 picoseconds for a 12 bit converter for a maximum sampling error of 0.5 of an lsb. These sampling aperture jitters are within the range of current hardware technology.

The stringent matching of the components in a conventional synchronous detector to obtain I and Q match within a receiver channel is avoided by the direct i-f conversion architecture. In addition, DC bias from the sampling circuitry is shifted out of the final signal pass band after digital filtering. Matching between receiver channels, however, is still a function of how well the individual A/D converters and SAW filters match.

The direct i-f conversion receiver eliminates the I/Q matching problem within a receiver. The increased sampling rate requirements on the A/D converter and T/H limit the effectiveness of the direct i-f sampler since the bandwidth and dynamic range limitation of current A/D converters, in most radar applications, usually limit system performance.

2.4 COMPONENT CONSTRAINTS ON DIGITAL BEAMFORMING PERFORMANCE

One of the requirements of a Digital Beamforming (DBF) is to provide very deep nulls against interference sources such as mainlobe or sidelobe jammers. The cancellation performance of a DBF array is determined in part by the jamming environment (number of jammers, effective radiated power, spacing and multipath conditions) and the imperfections in the components which make up the DBF array system. The component imperfections include phase errors, amplitude errors and non-linearities which limit the ability to form deep nulls in the array response over the entire signal bandwidth.

A method for evaluating component errors, for the purpose of creating error budgets for DBF receivers, is to analyze each error source in the receiver with respect to how it affects a factor known as the noise correlation coefficient. The noise correlation factor provides a direct assessment of the component with respect to the ability to cancel noise from a jamming source. The correlation factor also allows diverse kinds of errors to be translated into a single method of measurement which may be combined to yield a single measure of the effects of several different sources of errors in a DBF receiver. The noise correlation coefficient is a measure of the match between two receivers (or devices) when identical broadband noise is inserted into the two receivers. It is defined in terms of the residue power at the output of a subtractor following the two receiver channels.

The combined effect of several errors sources in a receiver is determined by computing the correlation coefficient for each of the errors and then taking the product of the individual correlation coefficients. The definitions for the terms used in

the expressions in the correlation coefficient analysis are covered in Appendix A. The analysis approach used in this section was performed by Mr. Sid Applebaum of General Electric on a contract with RADC-West[1] to determine the effects of channel-to-channel mismatch on the performance of mainbeam and sidelobe cancellation techniques which could be implemented by a DBF radar. Appendix A summarizes the results of Mr. Applebaum's analysis that are applicable to the DBSA contract. The remainder of this section is an application of Mr. Applebaum's approach to a typical array elemental receiver and includes all of the significant components from the LNA to the A/D converter output. No assumptions have been made about the digital beamformer that may be used with the array.

2.4.1 Analysis approach. In the following analysis, an error budget is constructed on the basis that the elemental receiver insertion amplitude and phase at the midband of each operating frequency will be compensated for by a calibration system. The error budgeting process is accomplished by calculating the contribution of the significant error sources, throughout the receiver, to the correlation coefficient for the entire receiver. The following is a list of the error sources considered in the budget:

1) RF section amplitude and phase mismatch.
2) RF section time delay mismatch.
3) Image filter out of band rejection.
4) IF section amplitude and phase mismatch.
5) IF section time delay mismatch.
6) Saw filter center frequency mismatch.
7) A/D converter sampling jitter.
8) A/D converter time delay match (aperture time).
9) A/D converter I and Q mismatch.
10) A/D converter spectral aliasing.

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[1]Mainbeam ECCM Task of "Surveillance Laboratory Support, Contract F30602-83-C-0017.

The remaining factors considered in the correlation coefficient budget are the receiver intermodulation product distortion (IMP) and correlated to uncorrelated noise ratios. The dynamic range computation model predicts the cumulative IMP distortion in the receiver from the third order IMP intercept points and the output signal levels of the analog components. The correlation coefficients for the third order IMP and noise components will be the composite value for the entire receiver.

In the following paragraphs, the rationale for choosing the correlation coefficients for each of the error sources will be discussed. The components used in the triple conversion receivers of a Digital Beamforming (DBF) array facility will be used as specific examples for computing correlation errors of typical components.

The phase and amplitude response of each receiver channel will differ because of insertion phase and amplitude differences in the components of each receiver channel. The overall insertion phase and amplitude out of each receiver channel is only compensated at the mid-point of the signal bandwidth at each operating frequency. There will, therefore, be residual phase and amplitude differences between receiver channels over the balance of the signal bandwidth due to differences in how the individual receiver components track over the signal bandwidth. It is convenient from an evaluation viewpoint to consider each component, that is a major contributor to residual phase and amplitude differences, separately when determining the overall correlation coefficient error budget. Equation A-7, from Appendix A, is used to convert the residual phase and amplitude deviations into the component correlation coefficient from component to component.

2.4.2 RF section amplitude and phase mismatch. The DBF 5.45 GHz C band image rejection filter has a phase and amplitude ripple across its 625 MHz agile bandwidth. Construction differences between filters result in small residual phase and amplitude deviations across the signal bandwidth.after the nominal filter phase and amplitude response at each calibration

frequency is subtracted out. The input image rejection filter is expected to have a 0.5 dB residual peak to peak ripple over its entire agile bandwidth; a 3 pole bandpass filter has been used (which results in approximately 3 cycles of phase and amplitude ripple over a 500 MHz bandwidth. The largest phase and amplitude changes occur at the band edge of the filter; using the nominal filter parameters, the amplitude change is about 0.107 dB over the last 11 MHz of this region. Over a 0.5 MHz signal bandwidth, the amplitude change is only about 0.005 dB; response differences between two filters could result in 20% difference in amplitude response or about 0.01 dB peak to peak difference. The phase change over the last 11 MHz of the agile bandwidth is about 3.266°. Over a 0.5 MHz signal bandwidth, the phase change is about 0.297°; response differences between two filters could differ by 20% in phase response or about 0.0594° peak to peak.

The correlation coefficient is based on the rms values of the amplitude and phase differences between filters. If the deviation in phase and amplitude between any two filters is considered to be uniformly distributed between the peak to peak deviations in the phase and amplitude slopes, the rms deviation is reduced by a factor of square root of 12 (0.003 dB in amplitude and 0.01715° in phase) over the signal bandwidth.

The residual phase and amplitude deviations between low noise amplifiers over the signal bandwidth are significantly smaller then the filter and therefore considered to be negligible.

The C band balanced mixer has an amplitude ripple of ± .5 dB across a 1.5 GHz bandwidth or 0.00033 dB variation across a 0.5 MHz bandwidth. The phase ripple is approximately 7° over the 1500 MHz or 0.0023° across the 0.5 MHz bandwidth. The worst case difference errors between two mixers occurs when their ripples are out of phase leading to peak errors twice as large (0.00066 dB and 0.0046°) as for one mixer. The rms value of the amplitude and phase ripples is 0.00019 dB and 0.00133 degrees.

2.4.3 First i-f section phase and amplitude mismatch. The first IF filter (2225 MHz) is a 3 section narrow band cavity filter. The 3 dB bandwidth of the filter is 20 MHz with an amplitude ripple of 0.5 dB peak. Over the 0.5 MHz signal bandwidth at the midband of the filter, the signal amplitude changes 0.0042 dB and the phase changes 0.167 degrees. Between two filters, the residual amplitude and phase deviation difference could be twice the individual deviations or 0.0084 dB peak and 0.334 degrees. The rms value of the small deviations is then 0.00243 dB and 0.0964 degrees.

2.4.4 First i-f section time delay mismatches. Filter insertion time delays vary with temperature; given that the filters must operate over a wide temperature range, it is desirable to minimize the filter insertion delay, where possible, and minimize temperature differences between the receiver channels. The time delay of filters, which are constructed from lumped constant devices, have an average change with temperature of about 0.01 percent per °C. The variation in time delay change with temperature is about 10% from filter to filter, the residual time delay variation is then only 0.001 percent per °C. The r-f section filter bandwidth is so wide that the filter delay differences are insignificant. The narrow 3 dB bandwidth of the first IF filter (20 MHz) makes it a significant contributor to receiver time delay. (The narrow bandwidth is required to reject a nearby image of the second mixer.) The 3 pole filter which will have a total time delay at midband of about 38 nanoseconds. The estimated time delay mismatch between filters, over an operating temperature range of -25 °C to +40 °C, is then:

38×10^{-9} sec x 10^{-5} sec per °C x 65 degrees C or approximately 25 picoseconds.

Individual modules in an array can have temperatures which differ by as much as 10 °C for typical flow rates of the cooling air. The time delay mismatch for this factor is equal to:

$38 \times 10^{-9} \times 10^{-4}$ sec per °C X 10 degrees C or approximately 38 picoseconds.

The worst case time delay differences between two filters is when the mismatched filters are also at different temperatures; the delay is then the sum of both or 63 picoseconds. Equation A-11 from Appendix A may be used to convert this time difference into its equivalent effect on the correlation coefficient. The correlation coefficient for the 0.5 MHz bandwidth is then 0.999999997 (-84.9 dB).

2.4.5 Image rejection. The mismatch error between receivers, in the image response region, will be modeled with the assumption that the phase and amplitude of any image output is completely decorrelated from receiver channel to receiver channel. Noise jamming at the image frequency of the receiver first down conversion is then decorrelated between receiver channels. If the image rejection filter has sufficient attenuation in the image frequency region, the decorrelated noise will have only a minor impact on subsequent processing of the receiver outputs. The image rejection of the receiver is normally specified in dB, hence, the image rejection can be directly translated into the correlation factor. A high first IF frequency is normally used to provide adequate separation of the pass region and rejection regions of the image reject filter. For the 2.225 GHz first IF frequency, the image response is -60 dB, hence, the correlation coefficient is 0.99999900 (-60.0 dB).

2.4.6 Second i-f section amplitude and phase mismatches. The first i-f balanced mixer has an amplitude ripple of 0.7 dB across a 1.2 GHz bandwidth or 0.000292 dB variation across a 0.5 MHz bandwidth. The phase ripple is approximately 7° over the 1200 MHz or 0.00292° across the 0.5 MHz bandwidth. The worst case difference errors between two mixers occurs when their ripples are out of phase leading to peak errors twice as large (0.000584 dB and 0.00584°) as for one mixer. The rms

value of the amplitude and phase ripples is 0.000169 dB and 0.00169°.

The major contributor to amplitude and phase mismatches in the second i-f section is the Surface Acoustic Wave (SAW) filter which sets the frequency response of the analog portion of the receiver module. A requirement for a rapid transition between the pass band and rejection band results in many tuned sections in the SAW filter to control the response shape; the pass band phase and ripple is typically closely spaced in frequency and difficult to correct. The match between filters that is practical to achieve in these high quality but low cost SAW filters is 0.15 dB peak to peak (.0530 dB rms) residual amplitude ripple and a 1.0° peak to peak (.354° rms) residual phase ripple. Equation A-7 from Appendix A may be used to convert the phase and amplitude residual ripple into the correlation coefficient. The correlation coefficient for the SAW filter phase and amplitude ripple is 0.9999244 (-41.2 dB).

2.4.7 SAW filter time delay & frequency mismatch. Since the SAW filters is the narrowest analog filter in the receiver, it also has the longest insertion delay. The SAW filter will have a longer time delay than that due to its bandwidth and response shape alone; the transducers are spaced by more then the minimum spacing required for the filter section to reduce other sources of coupling in the filter. The total SAW filter time delay will be about three microseconds. The time delay sensitivity to temperature change in the SAW filter is dependent on the substrate material that is used to build the filter. For Lithium Niobate SAW filters, the time delay temperature coefficient will be about 90 parts per million per °C. Tracking of the time delay coefficient between filters, however, is quite good (typically one percent) allowing the filters to operate over a large temperature range if there is only a small temperature difference between the SAW filters. Keeping the SAW filter out of the array can help to reduce the temperature range that the SAW is exposed to and make it easier to minimize temperature differences between filters.

The SAW filter insertion delay error will be modeled with a nominal insertion time delay of 3 microseconds and a 5° rms random temperature variation between SAW filters. This gives a time delay mismatch of 1350 picoseconds for a lithium niobate filter. When this time delay mismatch is used in equation 11 from Appendix A, the correlation coefficient for the 0.5 MHz bandwidth is found to be 0.999998501 (-58.2 dB).

The manufacturing tolerances on the center frequency match between SAW filters is about ± 0.04% peak or 0.0133% rms of the center frequency. For the 45.0 MHz IF frequency SAW filter, this corresponds to a frequency difference of 5.985 kHz or 1.2 % of the final signal band width. An approach to modeling the impact of the center frequency difference error is to consider that the mismatch produces an uncorrelated noise residue from the regions of the filter response where the two filters do not overlap each other. For the two 0.5 MHz rectangular frequency response filters, the responses can differ by 0.0133% times square root of 2 or 0.01881% in center frequency. For the 45 MHz IF frequency, this results in a correlation coefficient equal to 0.99971 (-35.4 dB down).

2.4.8 Synchronous detector mismatch. The synchronous detector has an amplitude ripple of 0.075 dB across a 5 MHz bandwidth or 0.0075 dB variation across a 0.5 MHz bandwidth. The phase ripple is approximately 0.4° over 5 MHz or 0.04° across the 0.5 MHz bandwidth. The worst case difference errors between two mixers occurs when their ripples are out of phase leading to peak errors twice as large (0.015 dB and 0.08°) as for one mixer. The rms value of the amplitude and phase ripples is 0.0053 dB and 0.028°.

The synchronous detector has a maximum amplitude unbalance of 1 dB maximum and a phase unbalance of ± 5° maximum over the 5 MHz video output bandwidth. Much of the synchronous detector error would be in the form of a residual bias; the amplitude and phase unbalance are corrected at the midband frequency leaving a potential error at other frequencies over the 0.25 MHz video bandwidth. Assuming that a quarter of the amplitude and phase

unbalance error is frequency sensitive, the amplitude error would be 0.025 dB and 0.25° maximum at the edge of the 0.25 MHz bandwidth video output. The rms amplitude and phase errors would then be 0.00722 dB and 0.0722° assuming a linear increase in the phase and amplitude errors.

2.4.9 Analog/digital conversion errors. Jitter in the A/D sampling aperture results in a difference in the correlation coefficient between two receiver channels. In the Analog Devices HTC 300 Track and Hold (which determines the jitter during A/D conversion), the sampling aperture jitter is specified to be 100 picoseconds. Equation 17, in Appendix A, gives the correlation coefficient for a rectangular filter. For a bandwidth of 0.5 MHz and 100 picoseconds aperture jitter the correlation coefficient is 0.999999995 (-82.6 dB).

The track and hold (T/H) amplifiers used in each receiver channel will have different aperture delays; thus, even with no time skew in the clock applied to individual receiver channels there will be fixed time skews in the output signal samples from each receiver channel. The manufacturer usually specifies the aperture delay of the T/H but not the variance in delay; the user must make his own estimate of what the variation is. Our experience has shown that the peak variation in aperture delays is frequently as much as 0.3 of the nominal aperture delays (30 nanoseconds for HTC 300 T/H). Taking the 30 nanoseconds as the ± 3 sigma variation in time delay, the rms variation between receiver channels is 5 nanoseconds. Using equation 17, in Appendix A, the expected correlation coefficient between receiver channels is 0.999986292 (48.6 dB) for a 5.0 nanosecond rms aperture error and the 0.5 MHz signal bandwidth.

A time delay trim in the clock circuit of the T/H amplifiers allows the I and Q outputs to be aligned within 1 nanosecond. The 1 nanosecond delay between the I and Q track and hold amplifiers introduces a frequency sensitive phase error between the I and Q samples of 0.09° at the edge of a 250 kHz video bandwidth or 0.026° rms phase error (the I and Q channel amplitudes

are unaffected by the time delay difference) the error results in a correlation coefficient of 0.999999784 (-66.9 dB).

After calibration, the gain of the Q channels is normalized to equal the I channel and the phase angle is corrected to 90°; the gain of each receiver is also normalized to a reference receiver. All of the gain and phase normalizations are relative the receiver responses at nominally the center of the signal bandwidth (at each operating frequency). The video amplifier and A/D converter frequency responses, however, will vary across receiver channels and between I and Q channels within each receiver. These gain differences will lead to decorrelation of any jamming noise input. The analog bandwidth of the channel is estimated to be 3.0 MHz with about a ± 10% variance in the response. The equivalent peak gain difference in each channel, at 250 kHz, is 0.073 dB and 0.48° in phase. The rms error between the I and Q components and between two channels is 0.042 dB and 0.28°; the correlation coefficient is then 0.9999953 (-43.2 dB)

The A/D sampling rate is 500 kHz, video noise components greater then 250 kHz will be aliased into the quantized pass band. The SAW filter output is specified to be more then 40 dB down 750 kHz away from the filter center frequency. The noise beyond 250 kHz, that is passed by the SAW filter is only partially correlated between receiver channels because of amplitude and phase differences between filters in their rejection region. It is estimated that the aliased noise power in the passband will be 50 dB below the signal in the passband; the aliased noise correlation coefficient is -50.0 dB (0.99999).

2.4.10 Dynamic range impact on noise correlation. The remainder of the receiver error budget is determined by dynamic range related factors. The three primary error effects related to receiver dynamic range are:

1) Receiver third order intercept (including A/D converter)
2) A/D quantization noise
3) A/D full scale voltage (saturation effects)

The derivations of the equations which show the impact of these effects is given in Appendix A. Representative values of the previous factors will be used to estimate the impact on receiver channel correlation.

Equation A-53, in Appendix A, shows the relationship between the third order intercept point and the operating level for the correlated (jamming) power signal. The Cancellation Ratio Limit (CRL) is equal to 20 log of the ratio of the third order intercept point to the power level of the noise less 7.782 dB. A 42.2 dB CRL (for example) requires a 3rd order intercept point 25 dB above the jamming power. This assumes independence of third order intermodulation products from one receiver to the next, which has been a good working model in the past.

The dynamic range of the analog portion of the DBF receivers is 53.2 dB, at the 1 dB gain compression point. At the 1 dB compression point, the third order intermodulation products are 20 dB down and the third order intercept point is 63.2 dB above the external noise level.

The 3rd order intercept point of the A/D converter is also a factor which impacts the CRL of the receivers. The full scale limit, for a sine wave input to the DBF receiver A/D converters, is 9.7 dBm. In a two tone test intermodulation distortion test, the peak amplitude of the sum of the two tones must be less then full scale; each tone must be restricted to 3.7 dBm in the DBF receivers. Intermodulation distortion test data has been taken on the Analog Devices HAS1002 1 MHz, 10 bit A/D converter with the HTC 0300 track and hold amplifier preceding the converter (the devices used in the DBF receivers). The 3rd order Inter Modulation Product (IMP) level was 46 dB below the output level of the two tones for nominal 50 kHz CW signals which were 6.5 dB below the full scale input for the converter. The total signal power input to the converter is then 9.7 dBm and the implied 3rd order intercept point is 32.7 dBm (46/2 + 9.7). (The typical definition for an analog device has been used for the A/D converter although the A/D converter is a hybrid analog/digital device.)

The third order non-linearities of the A/D converter, at a 9.7 dBm noise power input level to the A/D converter, would decrease the CRL to 38.2 dB (2 x 23 - 7.8). If the rms level of the noise power is at 9.7 dBm, the noise level is only 3 dB below the peak range of the A/D converter and many noise samples will be clipped when the A/D converter saturates. The A/D saturation significantly impacts the cancellation ratio of the receivers (discussed in section 2.3 of Appendix A). It is therefore necessary to reduce the noise power level at the A/D converter input to limit the number of noise peaks that reach saturation. Equation A-73 in the preceding section of the Appendix defines the overflow residue power generated by the A/D converter (relative to the noise power) for the ratio of the peak maximum bipolar quantizing voltage level to the noise power level. The accompanying table (Table A-6) in the Appendix shows that the noise power should be 10.8 dB below the peak A/D voltage to keep the saturation overflow power 40.6 dB down. The noise power level must therefore be decreased by 7.8 dB (to 1.9 dBm) to reduce the impact on CRL from clipping of the noise peaks; the decrease in the noise level raises the ratio of the third order intercept point to the noise level to 30.8 dB and hence the CRL would increase to 53.8 dB. Because of the large impact of clipping noise peaks, the A/D converter must be operated at a level at which the 3rd order intercept CRL is not the significant contributor to uncorrelated noise.

A/D differential linearity accounts for the fact that A/D converters are not perfect quantizers and there will be excess quantization noise beyond the "ideal" quantization noise. One method for describing the excess noise of the A/D is to specify the differential linearity relative to the least significant bit (LSB) of the converter. The differential linearity of the converter (typically equal to 0.5 of the LSB) is usually measured with a slowing moving input voltage which is equivalent to measuring the converter characteristics when quantizing DC. In many converters, the A/D converter noise output is significantly higher when quantizing signals at the frequency the specified sampling frequency would presumably support.

A more useful measurement of excess noise generated by the A/D converter (or the effective number of bits) is obtained by spectrally analyzing the A/D converter output when quantizing two equal power signals; the signals are adjusted to have a combined peak power less then the A/D saturation point and to be in the frequency range of interest. The noise power output from the converter is determined after excluding all coherent interference terms generated by the A/D non-linearities and normalizing the level by the integration gain of the spectral analysis processing.

In section 2.2 of Appendix A, the effects of A/D quantization and threshold noise are considered. As shown in equation A-57 in the Appendix, a 0.5 LSB differential lirearity will raise the quantization noise from the 1/12 of the quantization interval squared to 5/48ths of the quantization interval squared. When the external receiver noise is set equal to 1 LSB of the A/D converter, the "ideal" quantizer raises the effective noise level by 0.35 dB; when the differential linearity noise is considered, the noise level is raised by 0.43 dB. If the converter quantization noise level rises when the input frequency being quantized is raised, the effective number of bits is effectively reduced and higher quantization losses will be seen then shown here. The level of correlated spectral interference components also rise when the converter exhibits higher quantization noise with higher input frequencies; converters with such characteristics should not be used if their are alternative low noise A/D converters.

The dynamic range of the A/D converter will be specified in terms of the maximum jammer to noise ratio (JNR) that it can handle for a specified noise cancellation ratio. The starting point is the dynamic range of the ideal converter with a CW input signal and the external noise set equal to the LSB (noise sigma to q ratio of 1) of the converter. Equation A-79 in Section 2.4 of Appendix A shows that this reduces to just 6.02 (N-1) dB when the sigma to q ratio is 1. For a 10 bit converter, this dynamic range would be 54.18 dB.

The dynamic range of the converter must be reduced because noise clipping reduces the CRL. As discussed previously, it was necessary to reduce the jamming noise level to 10.8 dB below full scale to limit the overflow power due to noise clipping at -40.6 dB. The usable dynamic range of the converter is then 10.8 dB less then 54.12 dB or 43.4 dB. Finally the A/D differential non-linearity results in a 0.43 dB increase in the noise floor; the net A/D converter dynamic range is then 43.0 dB for the jamming power.

Table 3 summarizes all of the factors discussed in this section for the test bed receivers. The DBF receivers have 10 bit A/D converters and a 0.5 MHz signal bandwidth. The SAW filter center frequency mismatch is the largest contributor to the correlation errors shown in Table 3 because of the narrow bandwidth of the SAW filter. The bandwidth of the SAW filter could be increased up to 10 MHz (for wider band applications) without changing the filter center frequency; the center frequency mismatch error would then not be the limiting performance factor.

The correlation factor product compares the overall responses of two receiver channels and provides an estimate of the relative level of the noise residue after applying identical wide bandwidth noise to each receiver channel input and taking the difference of their outputs. Extending the correlation factor to an array, the array gain factor will reduce the effective level of the residue. In the case of a 32 element array with unit weighting on each elemental receiver, the array gain factor is 15.1 dB reducing the cancelled noise residue from -32.7 dB to 47.8 dB.

Table 3. Receiver correlation errors

Error source	Error magnitude (rms)	Correlation Factor	dB
RF image filter	0.0003 dB & 0.0175°	.999999906	-70.2
RF mixer	0.00019 dB & 0.00133°	.999999999	-89.9
First i-f filter	0.00243 dB & 0.0964°	.999997091	-55.4
IF filter time delay	63 picoseconds	.999999997	-84.9
RF image rejection	60 dB	.999999000	-60.0
First i-f mixer	0.000164 dB & 0.00169°	.999999999	-89.1
SAW filter	0.0530 dB & 0.354°	.9999244	-41.2
SAW time delay	1350 picoseconds	.999998501	-58.2
SAW freq. mismatch	0.0133% rms	.99971	-35.4
Synchronous detector	0.0053 dB & 0.028°	.999999389	-62.1
Detector I/Q mismatch	0.00722 dB & 0.0722°	.999997721	-56.4
A/D aperture jitter	100 picoseconds	.999999995	-82.6
A/D ch to ch delay	5 nanoseconds	.999986292	-48.6
A/D I/Q mismatch	1 nanosecond	.999999784	-66.9
A/D freq. sensitivity	0.042 dB & 0.28°	.9999953	-43.2
A/D noise aliasing	50 dB	.9999900	-50.0
	SUBTOTAL =	.9995974	-34.0
3rd order IM prod.	61.6 dB	.999995831	-53.8
A/D saturation level	10.8 dB	.9999129	-40.6
A/D dynamic range	43.4 dB (10 bits)	.9999543	-43.4
	TOTAL =	.9994605	-32.7

2.4.11 Calibration signal requirements. A calibration signal must be inserted into each receiver channel periodically to compensate for differential amplitude and phase drifts in the equipment. The calibration system compensates for insertion phase delay and amplitude differences in the receiver channels. Manufacturing costs can be reduced because LO distribution and signal cable do not need to be precisely trimmed to obtain electrical length matches and subassemblies do not require precision trimming and may be used interchangeably through out the system.

The signal to noise ratio (SNR) of the calibration signal at the receiver outputs must be high enough to permit the amplitude and phase correction factors to be accurately estimated; an insufficient SNR could lead to insertion phase and amplitude corrections that decrease channel to channel correlation. The calibration signal SNR may be improved by coherently integrating a longer time sample of the calibration signal. Long integration times may also be required to achieve sufficient signal to interference ratios when ECM is present.

Integration of the calibration signal to obtain sufficient SNR for a calibration measurement decreases the time available for normal receiver operations. In addition, the stability of the calibration signal source limits the gain enhancement that can be obtained by coherent integration. However, some noncoherent integration can be substituted for coherent integration to alleviate stability requirements in the signal source.

The accuracy of the calibration correction is ultimately limited by the accuracy to which the calibration signal phase and amplitude can be measured at the output of the calibration coupler in the receiver channel input. By measuring the insertion phase and loss of the feed network with a network analyzer and incorporating those correction factors in the processing of the calibration signal, the calibration system accuracy will be determined by the accuracy of the network analyzer. The network analyzer differential accuracy is sufficient to obtain the phase and amplitude matches required for a 50 dB correlation level.

2.5 ARRAY SELF CALIBRATION TECHNIQUES.

In the preceding analysis of channel to channel correlation, the insertion gain and phase of the receiver channels was assumed to be matched at the center of the signal passband for each operating frequency; hence, the insertion gain and phase errors were unbiased. Although insertion phase and gain corrections could be built into the receiver channels to eliminate bias errors at each operating frequency, many of the bias errors are sensitive to operating temperature, supply voltages and component aging. It is necessary, therefore, to incorporate calibration equipment into a DBF array to permit the insertion phase and gain corrections to be updated whenever operating conditions change. Ideally, the array calibration approach should account for all errors in the array components and have an inherent error significantly less then the maximum acceptable channel insertion phase and gain error.

The calibration technique which permits all component errors to be corrected is only achieved on an ideal pattern range or compact range facility with an equivalent far field source and an environment free of reflections and interference. The array calibration system, however, must be able to correct array transfer functions bias errors under field conditions with typical sources of interference and including non-ideal siting locations. Table 4 summarizes advantages and disadvantages of several calibration techniques for operational type array environments.

In Table 4, the two far-field calibration approaches permit the array radiating element characteristics to be included in the calibration. Both methods, however, are not suited to field equipment where frequent calibration is required. The airborne source is expensive to use and its angular position, relative to the array face, must be accurately known to derive phase calibration data. Suitable sites for a fixed far-field source are frequently not available at typical field sites; in addition, the need to enplace a far-field source as well as the DBF radar diminishes the radar mobility.

Table 4. Array Calibration Techniques.

Approach	Advantages	Disadvantages
Airborne Source	Includes array face environment. No added array complexity	Must accurately locate source. Logistically expensive.
Far-Field Source	Includes array face environment. No added array complexity.	Problems in siting source. Multipath effects. Not suitable for mobile DBF system.
Near-Field Source	Includes array face environment. No added array complexity.	Accurate source positioning required. Multipath effects.
Aperture Probe	Partial face environment. No added array complexity.	Accurate probe positioning required. Channel drift during measurement.
Aperture Face Coupling	Partial face environment. No added array complexity.	Large dynamic range required. Accuracy of end coupled data.
Precision Corporate Calibration Feed	Self-contained. High isolation between taps. Tap mismatch errors uncorrelated.	Array face errors not included. Calibration feed must be calibrated Questionable long-term accuracy.
Precision Element Loop Calibration Feed	Self-contained. Self-test of calibration feed ports. Self-compensating on port outputs.	Array face errors not included. Feed input must have low VSWR. Mismatch errors at port couplers are correlated.

The near-field source calibration approach also permits the array element characteristics to be included. The position of the source and the orientation of the array face relative to the source must be accurately known in order to compensate the array calibration data (for the near field phase front distortion) and be able to use the compensated data to correct the elemental receiver insertion gain and phase. It will also be difficult, in most cases, to find locations in a field environment for the source where there are not significant multipath effects.

The aperture probe calibration approach overcomes many of the previous limitations in siting of the source. A precision positioning system is required, however, to accurately place the probe over each element grid location for an insertion phase and amplitude measurement. The drift in the insertion phase and gain of a receiver channel over the time required to move the probe over the array to calibrate the overall array decreases the accuracy of any measurement. With the both the far-field and near-field sources, it was possible to simultaneously collect calibration data from all of the array elemental receivers which eliminates drift as a factor in the measurement errors.

In the aperture face coupling approach, an array auxiliary element (or possibly several) is used as the source to couple the calibration signal into the active elements of the array. Since the calibration source is part of the array, the approach eliminates the logistic problems of the external source approaches while seemingly including the array face environment in the calibration path. This calibration approach is subject to error, however, because the mutual coupling between elements drops off for elements not near the source element resulting in a large variation, across the array face, in the signal level input to the elemental receiver channels. The elemental receiver channels must have a large dynamic range to have sufficient signal-to-noise ratio to calibrate the receiver with the lowest mutual coupling and not saturate the receiver which has the highest mutual coupling. The dipole radiating element is particularly difficult to calibrate by the aperture face coupling calibration approach since mutual coupling is

relatively low for elements several wavelengths away. A second factor which decreases the accuracy of the aperture face coupling approach is that the test signal arrival angle is at end fire with respect to the array elements and not at the arrival angle which is normally used for forming the beams.

The two approaches using calibration feeds yield self contained calibration systems which can be accessed as frequently as needed when the array environment changes require a new set of calibration corrections (subject to operational constraints on time allocated for maintenance and calibration). The insertion phase and gain variations in the radiating element path, however, are not included in the calibration feed path which leaves a potential residual error in each receiver channel. It is imperative for low sidelobes that the radiating elements paths have essentially the same transfer function if there is no means of determining the variations in the radiating element path. The variations in the radiating element insertion phase and gain are reduced by close tolerances on the element size, position relative to the ground plane and array grid, and the dielectric properties of the materials making up the element (and radome cover); in addition, variations in the mutual coupling of the elements as a function of element location in the array are reduced by adding several rows and columns of dummy elements around the perimeter of the array to make the active element environmental more uniform across the array.

Even with the use of dummy elements and close control of the array radiating element construction and placement, the residual radiating element insertion phase and gain errors may be too large for desired level of sidelobes. It may be necessary to measure the transfer function of the radiating elements after the array is assembled and modify the calibration data measured for each elemental receiver by the complex array element transform to achieve the desired level of sidelobe control.

2.5.1 Precision corporate calibration feed. The precision corporate calibration feed has high isolation between the feed output ports; a reflection from a mismatch at the connection to

the monitoring port on the elemental receivers is attenuated by the isolation between feed ports and has minimal effect on any other port output. The distribution loss for the calibration signal through the corporate feed is equal to the splitting loss for the number of taps plus a small loss for the attenuation of the feed and cable interconnections. The construction errors in the corporate calibration feed distribution will be too high to use the feed outputs without compensation corrections to measure the insertion phase and gain of the elemental receivers of a low sidelobe array. Most applications will require a precision measurement of the insertion phase and loss of the calibration feed distribution (at each operating frequency) from the central input point on the feed to each receiver channel calibration input (including any cables on the output of the calibration feed). This will require, therefore, that the calibration feed system be measured after the feed system is assembled into an array so the measurements include the in situ insertion phase and attenuation all of the connections in the calibration path.

The corporate calibration feed has deficiency areas; an auxiliary calibration method is required to permit the calibration feed system to be monitored periodically. There must also be provisions, either through the feed system construction or a correction algorithm, to maintain accuracy over the operating temperature range. Differential phase errors may be avoided in the corporate calibration feed system by making all signal path lengths equal in length, have the same electrical sensitivity to changes in temperature and have a uniform thermal environment. Even though the corporate feed is composed of passive microwave components (assumes that the only amplifier is external to the feed), there is the potential for long term small changes in the feed losses and an electrical change at a coaxial connection due to some small mechanical disturbance. The calibration feed then may require recalibration of its transfer function from time to time to maintain system accuracy. In a large array with many calibration ports on a feed, the depth needed to fit the power dividers in may lead to a problem in the space available to fit the feed into the DBF array.

2.5.2 Precision element loop calibration feed. An alternative calibration feed concept, the precision element loop calibration feed, has features which eliminate some of the problems discussed in the previous paragraph. The essential features of the loop calibration feed are shown in Figure 4 which illustrates the feed applied to a row of an array. The calibration source has two paths to each elemental receiver coupling port (T_{ck}). The calibration feed ports utilize a non-directional single hole coupler, in a strip line feed implementation, to sample signals from the main transmission line of the feed; the coupling coefficient at a port is therefore identical from either path through the feed. Calibration of an elemental receiver channel requires two measurements with the loop calibration feed for each receiver channel. The calibration test signal output from the receiver channel must be measured with the test signal successively fed from each side of the loop feed. The complex vector product of the two measurements represents the transfer function for the receiver channel. The insertion phase and attenuation of the entire feed is included in each pair of measurements when the vector product of the two measurements is used. Variations in the location of the calibration test port and the phase shift and attenuation of the signal through the feed cancel out when the measurements to an output tap from each side of the feed are combined. The calibration measurements are insensitive to thermal expansion changes in the feed.

The loop calibration feed uses a single hole coupler for each receive element port. The single hole coupler consists of a small aperture in the ground plane above the strip line transmission line that passes through the length of the feed. Energy would normally be uniformly coupled from the main line into the region around the hole on the top side of the coupling hole defined by the space between the ground planes. The region above the coupling hole on the topside is modified, however by channel walls which create a waveguide region orthogonal to the main transmission line. The channel confines the coupled energy and isolates successive taps on the strip line transmission

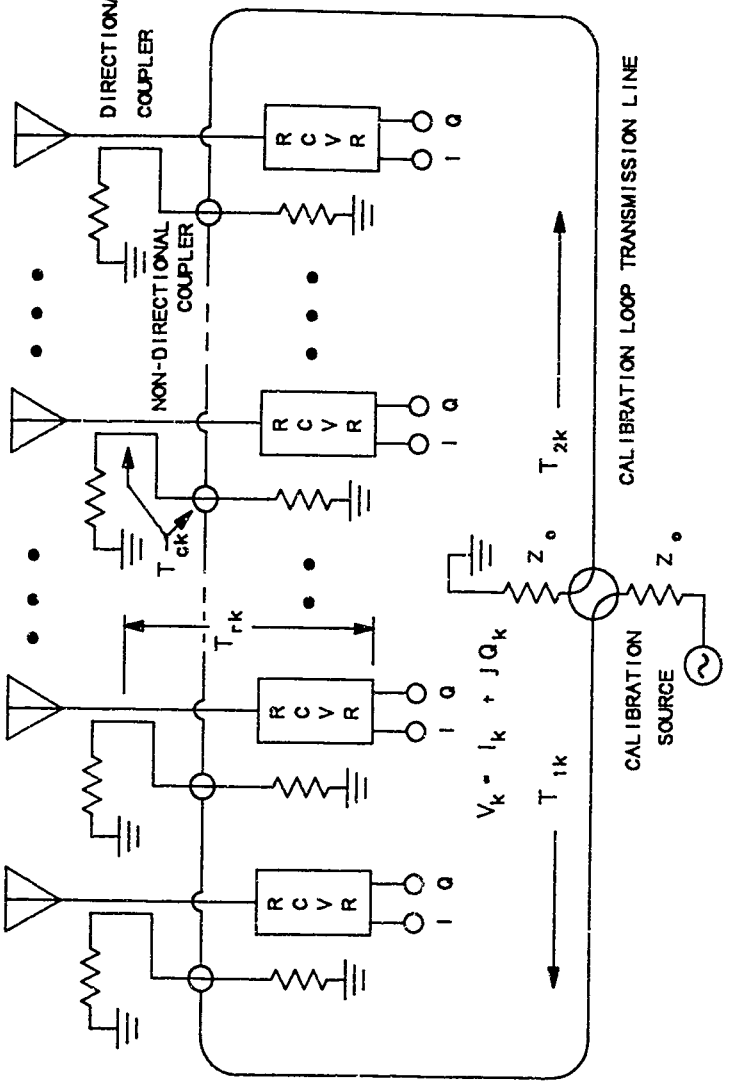

Figure 4. Element Loop Calibration Circuit

line. In the channel, energy is propagated in two directions towards an absorptive load and towards a strip line coupler which is the calibration output port. A low coupling loss in the non-directional coupler is desirable to minimize calibration signal attenuation and interference from signal leakage; a high coupling loss is desirable to minimize reflections from mismatches at the coupling apertures. A typical coupling value for the non-directional single hole coupler is -35 dB; the coupling on the calibration output port coupler is -20 dB. The total port insertion loss in the feed is then -55 dB plus a small loss for the energy coupled out of the other taps on the main feed line and the ohmic loss of the main strip line.

The calibration measurement at each port of the feed is accomplished by setting the calibration switch in the direction to propagate $V_{inc\ 1}$ (the signal entering the left side of the feed) and then simultaneously measuring all of the elemental receiver complex (I and Q) outputs (V_{k1}) for each tap. This is closely followed by the second set of measurements of the elemental receiver complex (I and Q) outputs (V_{k2}) for each tap, the calibration switch set to propagate $V_{inc\ 2}$ into the right side of the calibration loop. The desired elemental channel transfer function (T_{rk}) is proportional to the vector square root of the complex product of the measurements ($V_{k1} * V_{k2}$) and the port coupling constant K. The relationships between the measurements and the parameters of the loop calibrator are as follows (all terms in the expressions are complex quantities):

MEASURED VALUES

$$V_{k1} = V_{inc\ 1} * T_{1k} * T_{ck} * T_{rk}$$
$$V_{k2} = V_{inc\ 2} * T_{2k} * T_{ck} * T_{rk}$$

CALCULATED VALUES

$$A_k = V_{k1} * V_{k2}$$
$$T_{rk} = K_k * \mathrm{Sqrt}(A_k)$$

$$K1 = \mathrm{Sqrt}(V_{inc\ 1} * V_{inc\ 2})$$
$$K2 = \mathrm{Sqrt}(T_{1k} * T_{2k})$$

$$K_k = \frac{1}{K1 * K2 * T_{ck}}$$

The total port insertion loss (T_{ck}) is designed to be the same for each receiver port. The square root of the source voltage (K1) is a constant; the square root of the transfer function along the loop calibrator main strip line (K2) is independent of the port number. The calibration measurement is then (considering first order error effects) dependent only on having equal coupling through the single hole couplers and the calibration output port couplers.

The computation of the elemental channel transfer function (T_{rk}) requires taking a square root of the complex signal. The phase angle portion of the computation has a 180 degree phase ambiguity. The phase ambiguity is resolved by using the loop calibration measurements made from each side of the feed along with the calculated insertion phase. The loop calibrator introduces a phase gradient across the port measurements which is constant for any calibration frequency. The calculated phase angles are combined with the measurements made from one side of the feed; the combined data contains the expected phase gradient from using the measurements from one side. When the nominal expected phase gradient is subtracted from the combined data, the phase difference between successive channels should be constant. A 130 ° phase discontinuity means the wrong phase value (the ambiguous phase) was used from the computation of the elementary channel transfer function.

A calibration error will result if there are uncompensated differences between the couplers on each elemental receiver port. Another source of calibration error is associated with mismatches on the main transmission line; the signal reflected to the source from any mismatch on the transmission line also couples to the ports between the mismatch and the source because of the non-directional couplers. A mismatch at the load end of the loop calibration feed produces a correlated error across all of taps in the feed. The electrical distance of the tap spacing on the calibration feed, with typical elemental receiver

spacings, is about 3/4 of a wavelength. The reflection from the output end of the loop calibration feed takes the form of being a second (and much smaller) calibration signal with a different phase slope then the main calibration signal. After calibration, the second calibration signal results in a correlated sidelobe scanned away from the main beam position; the amplitude of the sidelobe is proportional to the return loss of the mismatch.

The second source of mismatched on the main transmission line is the individual non-directional couplers. The coupling hole introduces a shunt load consisting of a small capacitance, due to the magnitude of the coupling coefficient, in series with a load representing the two propagation directions in the channel. A shunt capacitance is also introduced by the coupling hole, the impedance of this load can be altered (including making it inductive) by matching circuits at the couplers. The mismatch at the couplers also produces a correlated error signal across the feed and a spurious sidelobe as in the case of the load end mismatch. An analysis of the loop calibrator and the effects of these errors appears in Appendix B.

2.5.3 Planar array loop calibrator. An extension of the loop calibrator to a planar array is shown in Figure 5. The calibration test signal for each row of the planar array is obtained from conventional power dividers. The power divider provides a calibration test signal which is approximately the same magnitude for all elements in the array. The receiver insertion phase and gain measurements for each row in the array are made in the same manner as described in Section 2.5.2. The insertion phase and gain differences between rows is determined by making a row to row measurement using a vertical loop calibrator. The vertical loop calibrator connects the calibration source to the center receiver port of each row calibration feed in the planar array. The receiver ports on the row calibration feeds are the cross channels which normally receive their signal inputs from the single hole coupler on the row loop strip line. The termination on the center receiver coupler port of the loop calibrator is omitted in order to accept an input signal which

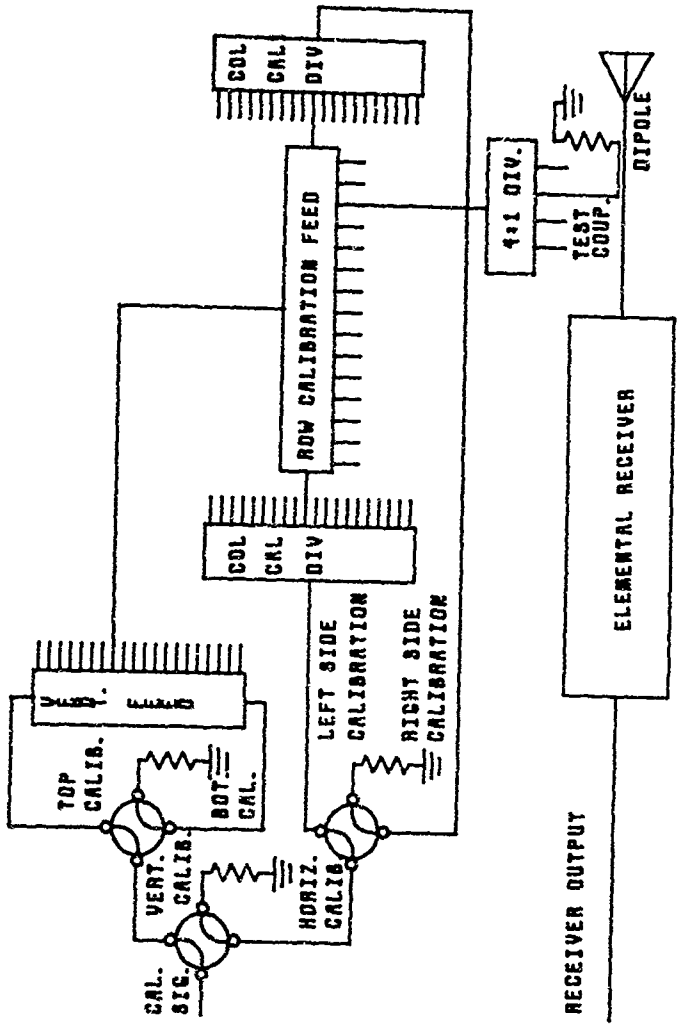

Figure 5. Pianar Array Loop Calibrator

is used in place of the normal row calibration signal during vertical calibration. The vertical calibration measurement provides a reference phase and gain correction value for the receivers connected to the center of each row loop calibrator which is used to normalize the transfer functions of the receivers at the centers of each row. After all the row calibrations are complete, the phase and gain corrections of each row can be combined with the vertical phase and gain corrections can be combined into a unique phase and gain correction for each receiver channel which allows all of the receiver channels insertion phases and gains to be normalized to the common reference.

2.6 IMPACT ON ARRAY PERFORMANCE OF RECEIVER BIAS ERRORS

The impact on array pattern measurements of uncorrected elemental receiver bias errors are considered in this section. The type errors considered include:

1) Uncorrelated DC offsets in the in-phase (I) and quadrature phase (Q) components of the elemental receivers.
2) I and Q gain mismatch and phase errors in a receiver.
3) Insertion phase and gain differences between receivers.

The effect of the previous errors will be considered with respect to the degradation in the sidelobe response of a 32 channel receive line array when measured with a CW source on an antenna test range.

2.6.1 Processing performed to obtain antenna patterns. The antenna response patterns of conventional antennas are typically measured with a CW source or a CW source modulated by a low frequency square wave. Since the recording equipment is usually equipped with a receiver with automatic frequency correction, the source frequency can be relatively unstable without significant impact on power type antenna patterns.

A CW source is also used to measure a digital beamforming (DBF) array receive patterns; there are, however, additional restriction on the source. The DBF receivers are designed to

use a phase stable LO source which is tuned to a discrete number of frequencies across the agile bandwidth. The antenna test range transmit source must be closely tuned to an operating frequency to obtain satisfactory array pattern data. The minimum requirement for tuning the source is to be aligned with the DBF operating frequency within 1/2 the matched filter bandwidth (assumes i-f filter sets signal bandwidth). Under minimum tuning alignment conditions, each time sample set from the DBF receivers must be coherently combined in a beamformer before successive time sample sets at the output of the beamformer can be non-coherently combined to increase the signal to noise ratio of the measurement. In the absence of a hardware beamformer, excessive processing time is required to use this approach for more then a few non-coherent samples.

If the source frequency can be accurately tuned to the DBF operating frequencies, the I and Q outputs of each individual DBF receiver can be separately accumulated (effectively a coherent integration of the CW signal by a filter matched to zero offset or DC) prior to forming the beams. This later case results in both a signal to noise enhancement and a narrower output signal bandwidth). The overall processing complexity is significantly reduced by this approach which makes it a desirable operating mode. The coherent integration mode is assumed for the following discussion.

The signal bandwidth of the example line array receivers is determined by a 500 kHz bandwidth SAW filter in the i-f amplifier; the I and Q outputs of the receiver synchronous detectors are sampled at a 500 kHz rate by 10 bit A/D converters. Sixty-four time samples of the 10 bit I and Q outputs are integrated for each receiver prior to the digital beamformer processing. The integration increases the signal to noise ratio of the pattern measurements and decreases the data rate into the beamformer processor by a factor of sixty-four. Unit weighting is applied to the sixty-four samples which reduces the 250 kHz video signal bandwidth to 7.8125 kHz before the beamformer and results in a sin(Nx)/sin(x) type amplitude response over the input bandwidth determined by the SAW filter; the sin(Nx)/sin(x)

sidelobes decay to -30.1 dB at 242.2 kHz (upper edge of the video bandwidth before integration). To minimize signal attenuation in the coherent integration filter, the pattern measurement frequency source must be within 2 kHz of the array operating frequency.

The pattern response of the line array is computed from the integrated outputs of the thirty-two DBF receivers, after the receivers responses have been normalized by calibration correction constants. The constants compensate the individual receiver outputs for I and Q amplitude balance, phase quadrature and DC bias errors due to phase and amplitude errors associated with the synchronous detector and A/D converter portion of the receivers. The calibration constants also compensate for insertion gain and phase differences between receivers. The normalization approach is the same when the DBF receivers are used in an operational approach with the exception that there is no integration prior to beamforming.

Amplitude weighting is also applied of the thirty-two phase and amplitude corrected receiver outputs during beamforming to suppress sidelobes. The Fast Fourier Transform (FFT) algorithm is used to combine the thirty-two receiver outputs and produce phase steered beams. The FFT algorithm provides uniformly spaced phase gradients over the range of ± 180 degrees; the individual outputs from the FFT processing correspond to beams uniformly spaced in T-plane space. A 256 point FFT transform is used in the beamforming processing to obtain intermediate samples of the array factor type antenna response. Each output from the FFT beamformer corresponds to a specific beam pointing angle; an array pattern response for a specific beam pointing angle is obtained by rotating the array past the r-f source and plotting the corresponding FFT output against the algebraic sum of the array mechanical pointing angle and the beam electronic scan angle.

2.6.2 Impact of receiver bias errors. The synchronous detectors, video amplifiers and A/D converters in each receiver channel are potential sources for DC bias errors in the I and Q

output of the receiver. There are several sources for the DC bias error in the I & Q outputs of a receiver channel and no known systematic error factors that would correlate the bias errors between receiver channels, the bias for the receiver channels will, therefore, be assumed to be guassian distributed with a zero mean. The factors which contribute to DC bias errors normally change at relatively slow rates (in the order of minutes). The I and Q bias from each receiver is, therefore, constant over the 128 microsecond period required to collect 64 samples with a 0.5 MHz A/D sampling clock. Coherent integration of sixty-four samples of the DC bias in each receiver channel increases the DC levels by a factor of sixty-four. Coherent integration of sixty-four samples of the external noise and A/D converter quantization noise increases the noise output level by the square root of the number of samples integrated (eight).

The r-f test signal used to characterize the array produces a DC output when the signal is exactly centered in the receiver bandpass. Coherent integration of the test signal will increase the signal level by the number of samples combined (sixty-four for the receive line array case). Since the processing gain for both the test signal and the DC bias of the receiver is the same in each receiver channel, no improvement is obtained in test signal to DC bias levels after integration. The ratio of the test signal to the receiver output noise level is, however, increased by integration; the gain is equal to the square root of the number of pulses which are coherently combined summed (by eight for sixty-four samples).

Thirty-two receiver channels are combined in the digital beamformer (FFT processor). The DC bias levels are considered to be uncorrelated from receiver to receiver; therefore, the integration gain for both the receiver channel DC bias and noise are the same or equal to the square root of the number of channels combined (square root of 32) for uniformly weighted signals from the receive line array. The test signal into the array is, however, correlated from receiver channel to channel. The output of the FFT beamformer which corresponds to pointing directly at the test source will be increased by the number of

receiver channels combined in the beamformer (thirty-two in the receive line array). The net gain for the test signal through the beamformer is then equal to the square root of the number of receivers that are combined (square root of thirty-two in the receive line array).

The receiver channel DC bias levels are determined during calibration, the residual DC bias levels remaining after calibration corrections are expected to be less than a fraction of an lsb of the A/D converter. A residual DC bias level will be a function of the accuracy of the determination of the bias and the frequency with which the estimate is updated. As indicated previously, the residual DC bias level from the receiver channels raise the effective noise level at the FFT beamformer output. Figure 6 is a plot of the mean value and 3 sigma value of the output noise level from the beamformer, after envelope detection, as a function of the rms DC bias level of the receiver channels. It should be noted that the plot is not normalized to unity gain for noise (noise output equal to the noise input); the plot shows the growth in noise level as a function of the ratio of the residual DC bias level to the quantization bit and includes the integration gain from summing 64 samples in each receiver channel and 32 receivers in the beamformer. For the plot, the external noise was set equal to the 2nd lsb of the A/D converter an operating point which results in only 0.09 dB signal to noise ratio loss due to the quantization noise from the A/D converter. The span of the residual DC bias level in the plot was zero to three times the external noise level. Figure 6 illustrates the significant degradation in the noise floor for any array measurements if the DC bias levels are not kept to fractions of a bit.

The DC bias level is statistically independent from receiver to receiver channel; the bias from a receiver channel is, however, highly correlated over time intervals of several minutes. If the residual DC bias levels from the receiver channels are high (after calibration), the noise in the antenna response patterns at the FFT beamformer output will be dominated by the residual DC bias levels. The response of each beamformer

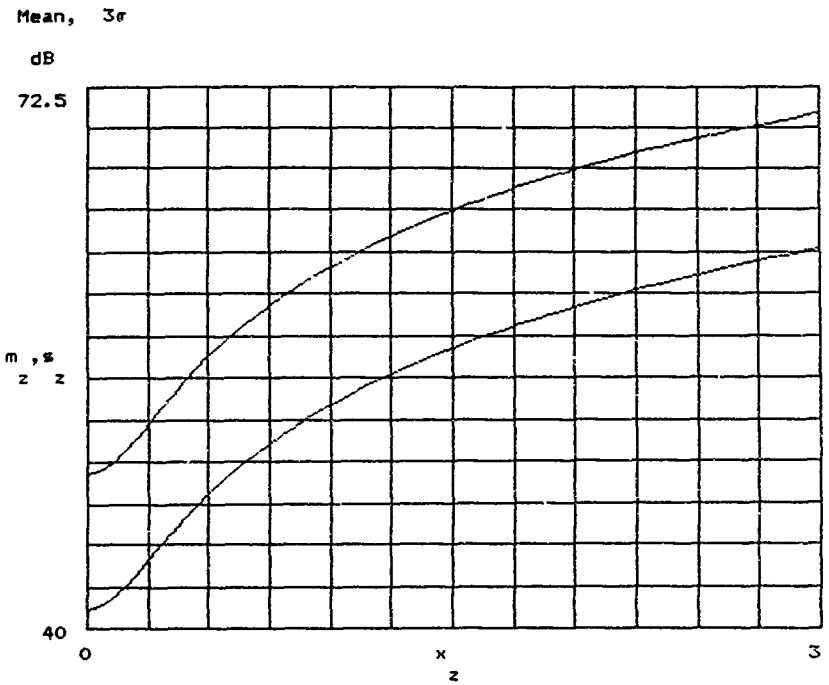

Figure 6. DC Bias Level At Beamformer Output

output will remain relatively unchanged over intervals of minutes because of the correlation of the DC bias levels.

Figure 7 shows the envelope detector statistical properties of the beamformer output for responses measured during the correlation period of the DC bias levels. The decrease in the three sigma variance in the beamformer response noise level (relative to Figure 6), when the DC bias level ratio is high, reflects that the noise in each receiver channel is dominated by the residual DC bias levels.

The largest CW test signal, that can be used with the 10 bit A/D converter without limiting, produces an output at 117.4 dB in Figures 6 and 7. If the DC bias levels of each receiver channel are fully corrected, the maximum output signal at the beamformer output will be approximately 76 dB above the mean value of the external receiver noise and 68 dB above the noise peaks. A residual DC bias level equal of only 0.5 of an lsb of the A/D converter reduces the antenna pattern dynamic range by 8 dB.

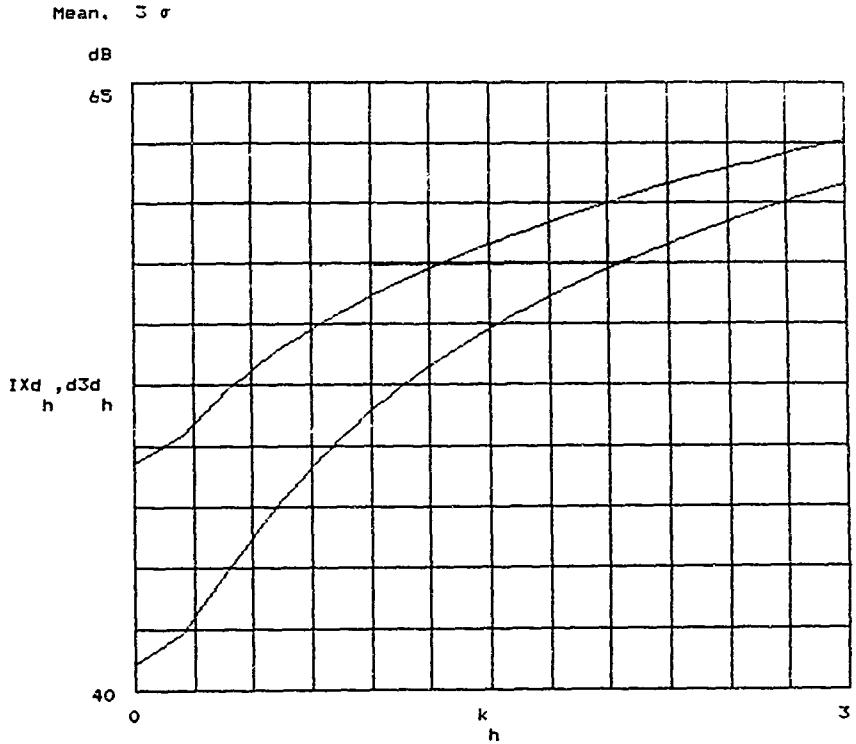

Figure 7. Short Term Noise Level From Beamformer

SECTION 3
IMPLEMENTATION PHASE

3.1 INTRODUCTION

The principal tasks accomplished during the implementation phase included:

1) Design, fabrication and test of a subarray element and a thirty-two element line array.
2) Fabrication and test of a unique "loop type" calibration feed for the thirty-two element array.
3) Fabrication and test of thirty-two elemental C-band receivers with A/D converters and an LO system.
4) Design, fabrication and test of a recording system to enable calibration and detailed pattern measurements of the thirty-two element test bed array.
5) Implementation of control software to permit calibration of the array and collection of pattern data on an antenna test range.

The specification for the DBSA test bed thirty-two element line array hardware has been adapted from the design of a digital beamforming line array developed by General Electric for its multistatic digital beamforming radar (DBR) test facility. The elevation beam width is the major difference between the two arrays. The DBR array is required to have a large elevation beamwidth to span the volume illuminated by the multistatic transmitters. The DBSA line array is intended to be used in digital beamforming studies that include extensive measurements on an antenna test range. A narrow elevation beamwidth is needed in the DBSA application to minimize interference from reflections during array testing.

The interface with the A/D converter outputs is also different between the DBR and DBSA arrays because of their different applications. The DBSA array is interfaced to an HP9836 desk top computer which is part of the test equipment at the RADC Ispwich, Ma. antenna test facilities. The computer

controls the collection of the data from the DBSA array and the position of the array rotator.

The computer is also used to process the thirty-two channel receiver outputs from the array. The processing includes: calibration, data correction and digital beamforming. Calibration weights for each receive channel are computed from the calibration waveform outputs. The calibration weights are applied to subsequent receive data to correct for errors in insertion phase and gain, DC offsets and I/Q unbalance. An FFT algorithm is used to form simultaneous beams from the receive data stored during a pattern measurement. The operator may select the scan range of the array rotator over which the pattern data is collected. The digitally formed beam sets are reprocessed, for an operator selectable beam position, to create conventional antenna response patterns of output power level versus azimuth angle.

A thirty-two element line array antenna, thirty-two elemental receiver channels with LOs, and a data recording control unit were fabricated based on the equipment specification defined in the study phase. The agile bandwidth of the triple conversion elemental receivers is 5.2 to 5.7 GHz; the signal bandwidth is 500 kHz. A pair of 10-bit A/D converters, clocked at 500 kHz rate, are used in each receiver channel to quantize the in-phase and quadrature phase (I & Q) outputs of the receiver synchronous detectors. A loop type calibration feed is used in the DBSA array.

The receive element subarray of the test bed array consists of 8 vertically polarized, strip line dipole elements. A dummy dipole is present on each side of the 8 dipoles. The eight active elements in the subarray are combined in a corporate power combiner with unit weighting on each tap. The thirty-two array elements are spaced at 0.51 of a wavelength at mid-band.

The characterization of the digital beamforming test bed array and evaluation of digitally formed beam algorithms are being performed by members of the staff of the Electromagnetics Development Directorate of the Rome Air Development Center at Hanscom Air Force Base, the sponsors of the DBSA contract.

3.2 DBSA REQUIREMENTS

The Digital Beamforming Steering Antenna (DBSA) test bed array antenna is required to demonstrate the feasibility of self calibration, in a digital beamforming system, as a means of achieving pattern control over large bandwidths and dynamic range in radar and communication antennas intended for demanding tactical environments. The DBSA is intended to demonstrate techniques which are applicable to antennas with 30-40 dB of aperture gain and lower than 50 dB sidelobe levels.

The array self calibration techniques are required to be consistent with various pattern control functions including: open and closed loop adaptive null steering in sidelobe areas and in the main beam, very low sidelobe antenna pattern formation, or real time sidelobe control by varying aperture weighting. The pattern control should be achieved with jamming to self noise level (in an elemental receiver with a single dipole element) greater then 30 dB for tactical stand off jamming environments.

The DBSA approach must be applicable to instantaneous bandwidths that would be used in radars such as advanced tactical surveillance radars; however the test bed equipment is not required to incorporate wide bandwidth A/D converters and calibration speed can dictate system bandwidth.

3.3 TEST BED ARCHITECTURE

The DBSA was constrained to 32 elemental receivers because of implementation cost issues. Since th objective of the program was to investigate the effectiveness of self calibration techniques to provide high quality beams and control of beams through digital beamforming, it was necessary to select a configuration for the elements that optimized measurement of low sidelobes.

A two dimensional configuration of 32 elemental receive elements, such as a 4 element high by 8 element wide array, leads to low resolution in both planes and limited sidelobe suppression capability; this limits the capability to measure array sidelobes because of the susceptibility to multipath

interference and limited useful data on array accuracy errors due to the broad beamwidths (12.7° by 25.4° in an unweighted array with elements spaced on half wavelength). Further the low array gain of only 20.0 dB limits system sensitivity. The array beamwidths may be reduced (and the array gain is increased) by spacing the elements further apart. The loss in scanning range and departure from typical element spacings would make the test results atypical of most potential digital beamforming applications making the increased performance of negligible value.

The array beamwidths may be decreased without increasing the number of elemental receivers by using subarrays. As an example, 4 elements may be combined in elevation increasing the aperture size by a factor of 4 and allowing the beamwidths to be reduced in both planes; with a 8 element high by 16 element wide array, the unweighted beamwidths would decrease to 6.35° by 12.7° and the gain would increase to 26.0 dB, with elements spaced on a half wave length. With 16 elemental receivers in the horizontal plane, sidelobe evaluation would be enhanced and a full range of electronic scan angles could be utilized. The subarraying of 4 elements in the elevation plane, however, significantly limits performance in that plane because of the grating lobes created by the subarrays. With only two elemental receivers in the elevation plane, there is no useful way of applying elevation amplitude weights in the digital beamformer; the subarray combiners, however, could incorporate fixed weighting to provide an elevation taper for sidelobe control. With only two subarrays and fixed weighting in the elevation plane, amplitude quantization sidelobes would not be present in the elevation plane. The subarrayed elements would however produce significant phase quantization sidelobes when the array is scanned in elevation. With amplitude weighting on the subarrays the subarray pattern will be broaden and the cancellation of the grating lobes at ±30° will be reduced increasing sidelobes even with small scan angles. The expected value for the array grating lobes as a function of the subarray

parameters has been covered in the literature.[2] The sidelobe performance in the elevation plane and the scanning capabilities are limited by the use of subarrays. With only 32 active elements in the array, there is limited performance value and significant dilution of the array measurements to use an array configuration that scans in both planes.

The final configuration considered was a horizontal line array of the 32 elemental receivers with fixed subarrays in elevation to reduce the elevation beamwidth. This provides the most effective utilization of the receivers for digital beamforming measurements.

3.4 TEST BED PARAMETERS

The parameters of the DBSA equipment are given in Table 5. A dipole is used for the subarray radiating element. The dipole elements are spaced 1.75" apart in the vertical plane and 1.10" in the horizontal plane; the horizontal spacing will support an azimuth scan of ± 55° over the frequency band. The elevation beamwidth is established by a subarray of eight vertically polarized dipoles; the eight dipoles are combined in a uniformly weighted power combiner. A terminated dummy dipole is added at each end of the eight dipoles to decrease the variation in mutual coupling across the subarray.

Thirty-two receivers and the local oscillators to run the receivers are part of the test bed hardware. The receivers include I and Q synchronous detectors with 10 bit I & Q digital outputs sampled at 500 kHz rate. The I & Q data outputs are collected in sample batches in a hardware buffer which can store up to 256 samples from each receiver. A hardware sample integrator on each I & Q output from the 32 re- ceiver channels sums 64 samples in the pattern mode to reduce the data rate to the computer and to enhance signal to noise ratio.

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[2]Mailloux, Robert J., "Array Grating lobes due to Periodic Phase, Amplitude, and Time Delay Quantization" IEEE Transactions on Antennas and Propagation, Vol. AP-32, No. 12, pp. 1364-68, December 1984.

The built in calibration system permits measurement of the individual receiver channel critical alignment parameters and calculation of correction weights. The calibration corrections are accomplished as part of the pattern data processing in the HP 9836 computer.

Table 5. Test Bed Parameters.

ARRAY PARAMETERS	
Frequency Band	5.2 - 5.7 GHz
Array Type	32-element line array + 4 dummies
Array Element Type	8 dipole column + 2 dummies
Broadside Az. HPBW	4.2° (35 dB sidelobe taper)
Elevation HPBW	7.9° (Uniform taper)
Azimuth Scan Capability	± 55°
RECEIVER PARAMETERS	
Receiver Type	Triple-conversion, frequency agile
Image Rejection	50 dB
Frequency Tuning	Twenty-six frequencies across band
Short Term Stability	1×10^{-9}
Instantaneous Signal BW	500 kHz
Noise Figure	4.5 dB
Dynamic Range	42 dB
A/D Converters	10-bit I and Q
Sampling Rate	0.5 MHz
A/D Operating Point	RMS noise to quantizing bit = 2
Phase Mismatch	< 2° RMS
DC Offset	1/4 LSB
I & Q Delay Mismatch	<20 nanoseconds
Calibration Method	Self-calibrating bilateral loop including synchronous detectors

Table 5. Test Bed Parameters cont'd.

RECORDING AND CONTROL SUBSYSTEM	
Pattern Data Buffer	256 I & Q words x 32 channels
Sampling Interval	20 milliseconds minimum sampling interval
Pattern Integration	64 I & Q sample pairs
Data Interface	HP-IB interface to HP 9836 computer
CALIBRATION SYSTEM	
Channel Factors	I & Q channel DC bias
	I & Q amplitude balance
	I & Q phase quadrature
Cross channel Factors	Insertion phase match
	Insertion gain match

3.5 IMPLEMENTATION APPROACH

The self-calibration approach used in the DBSA equipment provides a means of accommodating to variations in the transfer function of all the circuitry between the calibration reference point and the digital I & Q outputs of the elemental receiver channels. Variations in the transfer function of the circuitry preceding the calibration point in the array, being outside the calibration loop, will diminish the control over array sidelobes that can be accomplished with self-calibration. Figure 8, the DBSA System Block Diagram, illustrates the relationship between the major assemblies which make up the DBSA equipment.

The dipole subarray and the interface to the calibration feed are outside of the calibration loop and therefore had critical design tolerances. The dipole subarray, including the dipole elements and the r-f power combiner were implemented as a single strip line assembly to assure uniform performance between subarrays. The strip line transmission lines and couplers which make up the calibrator assembly were housed in a precision machined frame to control assembly tolerances and signal leakage

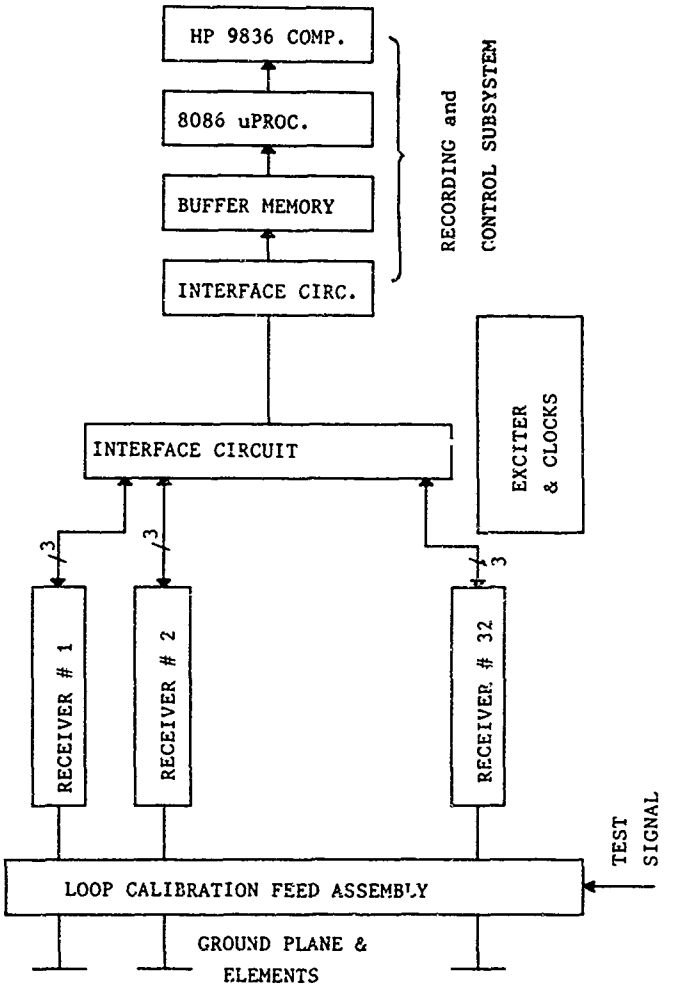

Figure 8. DBSA SYSTEM BLOCK DIAGRAM

between adjacent calibrator taps. The subarray elements, the array ground plane and the calibrator were designed as one assembly and relied on direct connection of the subarray to the calibrator, without the use of coax cables, to reduce insertion phase variations.

The elemental receivers, which includes all of the receiver circuitry from the low noise C-band r-f amplifier to the A/D converter serial output registers, were implemented as individual single interchangeable assemblies. The exciter assembly used phase locked synthesizers and a common 5 MHz reference source to generate all of the LOs used in the system (agile C-band LO, fixed LO for the 2nd i-f and synchronous detector reference frequency). The A/D sampling clock was also derived from the 5 MHz reference source. Only passive r-f power dividers were used in the LO distribution to minimize phase and amplitude fluctuations between receiver channels; all power amplification preceded the power dividers. Insertion phase and gain variations introduced by the LO system are cancelled out by the calibration system. The LO system, therefore, did not require any precision components allowing commercially available r-f power dividers to be used in the distribution system.

The interface between a digital beamforming elemental receiver array and the balance of the radar processing equipment includes many more connections than a conventional array. In most radar applications, it is desirable to separate the array from the other portions of the radar. It is also desirable to minimize the hardware included in the array enclosure because it is subject to extremes in temperature and sun loading in an operational environment. In addition, the access to the array equipment is usually more difficult because of its mounting location and the need to preserve environmental protection. When the separation between the array circuitry and the balance of the radar equipment is long (>20 feet); it is desirable to have only low frequency signals in the interface cables to minimize signal attenuation and reduce the frequency sensitivity of reflections on the transmission line. It is undesirable, however, to have base band video signals in the array interface

connections because of the difficulty in isolating the signals from noise interference near DC and the power line frequencies. The last i-f frequency is than the lowest analog frequency which can be used in the array interface without special circuitry to cancel noise interference.

A digital interface can be made between the array and the rest of the radar when the A/D converters are included in the array equipment; the digital signals are less vulnerable to noise and interference pick up than the base band video is. The lowest bandwidth interface, a parallel output, requires many more connections than the analog interface. With 10 bit A/D converters, for example, there are 20 connections per channel as opposed to 1 connection when an i-f interface is used. If a serial output is used at the interface, the number of interconnections can be reduced to one per channel if the clock rate needed to transfer the I and Q outputs on the same output does not become excessive. In the DBSA configuration, the A/D converter sampling rate is only 0.5 MHz which requires a minimum transfer rate of 10 MHz on the serial output.

In Figure 8, the Recording and Control Subsystem has 32 serial inputs from the array corresponding to the 32 elemental receivers. Signal data from the array is collected in contiguous blocks of 256 or 64 samples depending if the data is to be used for array calibration or for array pattern measurements. The instantaneous data rate from the array is 48 Megabytes per second (byte equals 8 bits, 3 bytes required for each I & Q pair collected from each receiver). The HP 9836 computer used to process the array data can not accept data at a 48 Megabyte rate and requires an external buffer memory to retain the data block and output at the channel rate that the computer can accept (about 300 Kilobytes per second).

3.5.1 Subarray element design. The subarray dipole antenna consists of eight vertically polarized dipole elements spaced on 1.75 inch centers. The dipoles are fed with a uniform amplitude, equal phase Wilkinson power divider circuit. Each

vertical subarray dipole element includes a dummy dipole at either end for impedance stabilization.

The dipoles are implemented as straight-arm dipoles on a copper clad Duroid substrate (Figure 9). Dipole patterns are etched on the outer sides of a two piece strip line circuit; on the inner surface of one substrate, a center-conductor loop is etched to feed the dipoles. A single section impedance matching transformer is etched into the center conductor between the dipole and Wilkerson Power Divider. The transformer was designed to minimize the active VSWR of a dipole element over the 5.2 to 5.7 GHz operating band for the scan range of 0 to 40 degrees in the H-plane. The transformer design is based on measurements made on a 7 dipole E-plane simulator; the measurements included the passive impedance of the central element and coupling between the central element and its neighbors for a uniformly weighted array.

The E-plane simulator consisted of 7 dipoles spaced 1.1 inches horizontally and ground planes spaced 1.75 inches above and below the dipoles to simulate coupling between the columns of the dipoles. The predicted active impedance of the element, using the transformer, was 1.66:1 over the scan range with the VSWR at 50° scan angle being less than 2.5:1.

The test model of the 8-way Wilkerson power divider had amplitudes equal to within 0.1 dB over the band and phases equal to within 1.5° (typically) with a worst case of 3°. The return loss on the common port was greater than 28 dB with the output ports terminated.

3.5.2 Calibrator design. The loop calibrator, described in section 2.5.2 and Appendix B, was used for the array calibrator. Figure 10 is a schematic of the 32 port calibrator used in the DBSA array. The thirty-two active array elements are coupled to the elemental receivers through the direct connection ports. The calibration signal path from the loop calibrator to a receiver input contains two couplers. The first coupler is a 30 dB non-directional coupler. The coupling holes through the ground plane at the intersection of the calibration loop feed

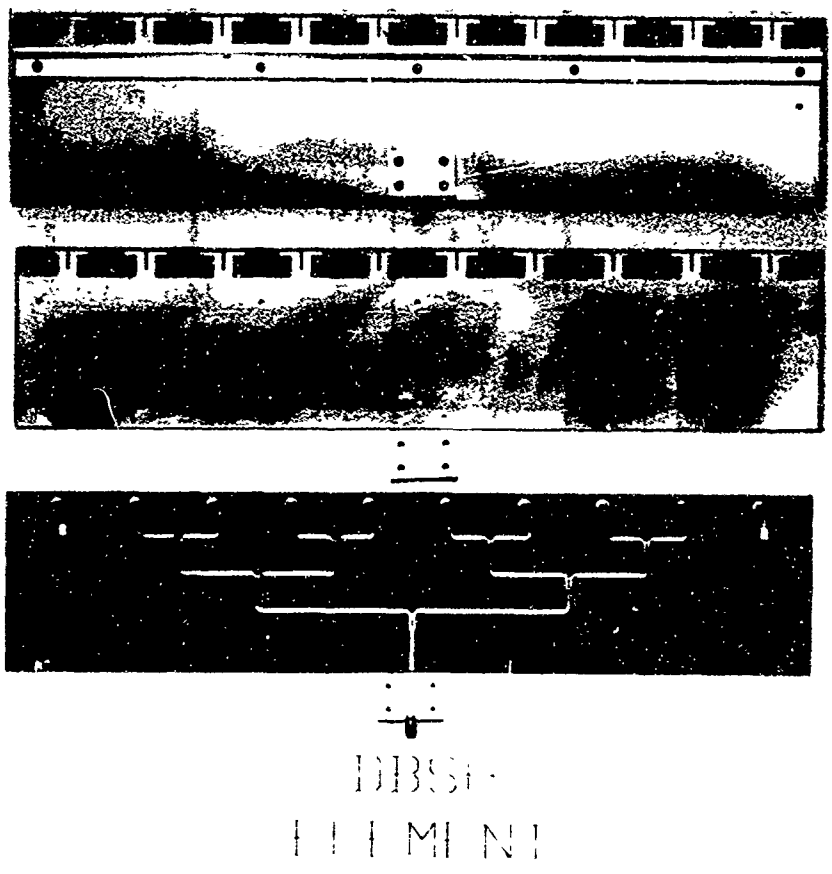

Figure 9. DBSA Element Components

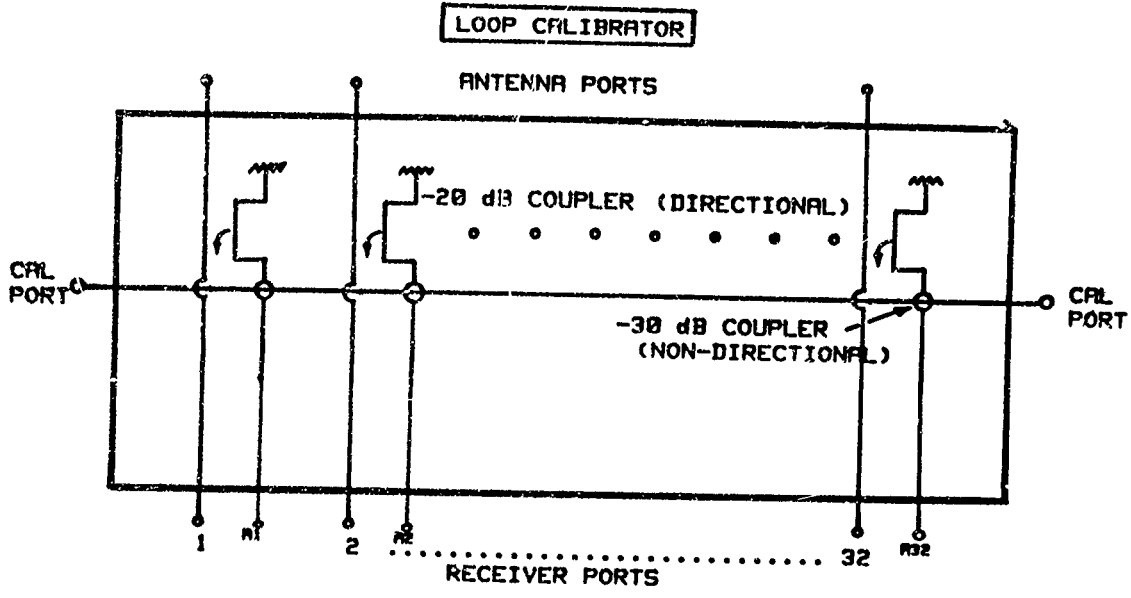

Figure 10. Loop Calibrator Schematic

line and the cross lines labeled A1-A32 couples energy into the cavities that surround the cross lines. The second coupler is a 20 dB directional strip line coupler on the antenna to receiver interconnection strip line.

The "A" ports of the 20 dB coupler line are terminated external to the calibrator feed to provide access to the signal coupled from the calibration loop; the "A" ports are called the "auxiliary" outputs of the calibration feed. The opposite end of the 20 dB strip line coupler is terminated within the calibration feed.

The strip line circuit runs for one port of the calibration feed are illustrated in Figure 11. The non-directional coupler is the coupling hole at the cross over of the calibration line and the auxiliary calibration line. The 20 dB coupler includes tuning "fingers" which compensate the coupler for differences in the propagation constant for the forward wave and backward wave.

Test results on a single non-directional coupler showed a maximum VSWR of 1.1 across the 5.2 to 5.7 GHz. The directivity of the 20 dB directional couplers was greater than 25 dB across the same band. For the 32 port loop calibrator, the worst case rms amplitude and phase error was 0.26 dB and 2.46° across the frequency band of 5.2 to 5.7 GHz.

3.5.3 Receiver design. A triple conversion receiver was used to provide good image rejection. Figure 12 is a block diagram of the elemental receiver. The receiver specifications are shown in Table 6.

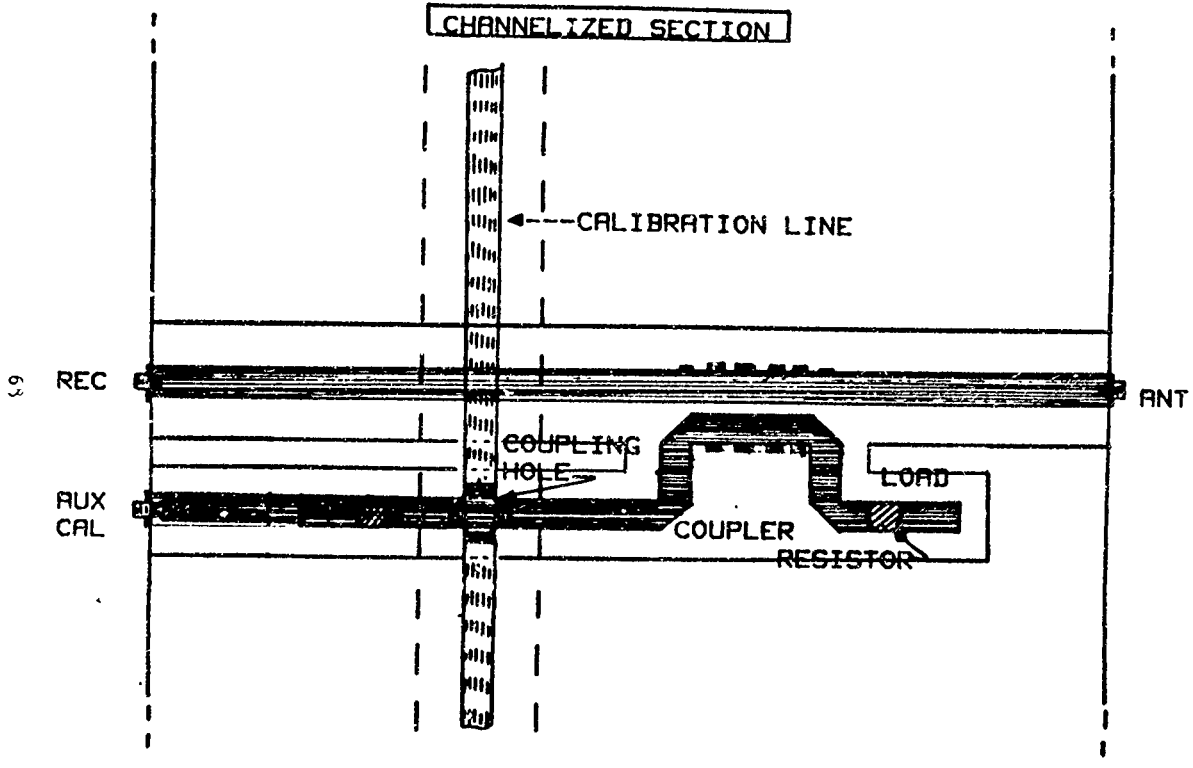

Figure 11. Loop Calibrator Strip Line Circuits

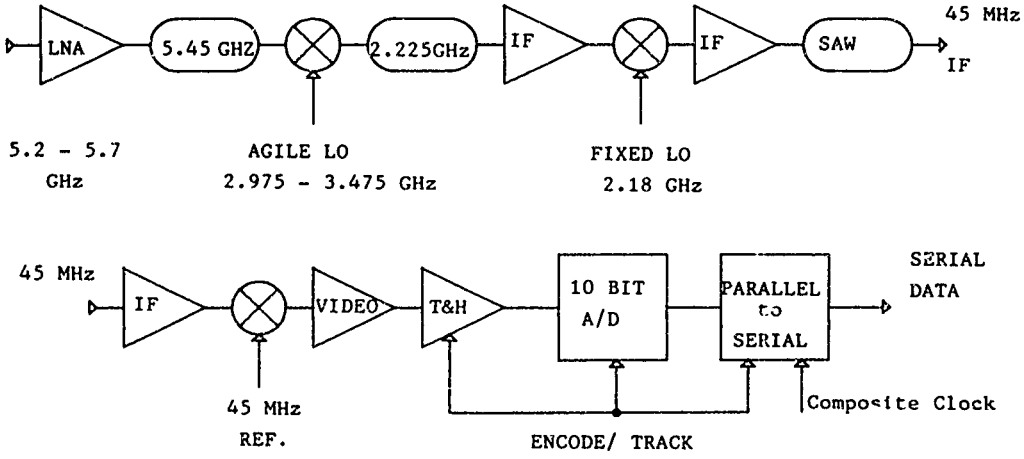

Figure 12. Elemental Receiver Block Diagram

Table 6. Receiver Specifications.

Frequency Coverage	5.2 to 5.7 GHz in 20 MHz steps
Signal Bandwidth (3 dB)	500 kHz
Receiver Noise Figure	4.1 dB
Image Rejection	50 dB
Gain Tolerance	± 1 dB
Dynamic Range	40.8 dB
A/D Converters	10 bit I and 10 bit Q
A/D operating Point	RMS noise at 2 LSBs
A/D Conversion Rate	500 kHz
Digital Data Output	Serial - single ended
Maximum r-f Input	0.5 watt average, 100 watt peak
Physical Size	4.5" x 1" x 31"
Power Dissipation:	13.0 watts per receiver

Dynamic range is specified in terms of the level of the cumulative third order intermodulation products when two equal amplitude signals are present at the receiver input and the peak voltage into the A/D converters is at full scale.

A C-band low noise amplifier (4.0 dB noise figure) with 27 dB gain sets the overall receiver noise figure of 4.1 dB at the A/D converter input. The C-band image rejection filter has a 3 dB bandwidth of 625 MHz and a 30 dB bandwidth of 1600 MHz maximum. The in-band amplitude ripple is 0.5 dB peak; over a 0.5 MHz bandwidth, the difference in amplitude and phase response between receiver channels is, however, negligible when the insertion amplitude and phase is cancelled out at each operating frequency.

A high intercept point (+20 dBm), double balanced mixer was used for the first down conversion mixer. The 2225 MHz first i-f frequency places the image (750 to 1250 MHz) well outside the amplifier pass band. A narrow band cavity type bandpass filter was used for the second i-f image rejection filter; these high Q filters permit very narrow bandwidths to be realized without excessive insertion loss. The 3 dB bandwidth of the 2225 MHz center frequency filter is 20 MHz with only 2.2 dB

insertion loss; the in-band amplitude ripple is 0.5 dB peak. The narrow band cavity filter permits the third i-f frequency to be optimized for the final filter bandwidth of 500 kHz since the image frequency (2135 MHz) will be rejected by the filter.

A third i-f frequency of 45 MHz was selected since it was favorable for realizing the 500 kHz bandwidth final receiver bandwidth. The third i-f bandpass filter is the most critical analog component because its response has the most impact on channel to channel response match. A SAW filter was used for this filter because of the consistency in transfer function which can be achieved in this technology. Table 7 list the performance specifications for the SAW filter.

Table 7. SAW filter Specifications.

Center Frequency	45 MHz ± 0.04%
Temperature Coefficient	± 0.01%/°C
Bandwidth: 1 dB	300 kHz
3 dB	500 kHz ± 0.1% unit to unit
40 dB	1.5 MHz or less ± 1% unit to unit
Ultimate Rejection	70 dB
Amplitude Ripple	0.1 dB peak (in-band)
Insertion Loss	20 dB ± 3 dB (± 1 dB unit to unit)
Phase Match	1° peak unit to unit

The SAW filters were supplied by Sawtek; the response match of the filters was checked on 4 pairs of filters by passing 10 MHz noise through pairs of filters and measuring the noise residue present at the output of a subtractor circuit which combined the filter outputs. The residue from the subtractor output was measured after trimming out the static insertion phase and loss differences between the two filters. The insertion phase and loss trimming is comparable to the static correction made to the overall receiver transfer function after calibration. The average residue across the noise bandwidth was 40 dB which is better than the 35 dB allocated for the entire receiver.

An integrated synchronous detector assembly was used for the I and Q phase detectors. The assembly included an in-phase i-f signal power divider, a 3 dB quadrature hybrid for the reference frequency and the I and Q mixers. The I & Q balance of these devices is within ± 5° of phase quadrature and 1 dB in amplitude balance over a video bandwidth of DC to 5 MHz. The static amplitude and phase errors of the synchronous detector are measured during calibration; correction coefficients are computed to correct subsequent receive channel I & Q outputs.

Analog Devices HOS-050A high current output, wide band video amplifier (100 MHz gain bandwidth product) was used on the output of the synchronous detectors to obtain the voltage swing of 7.5 volts which his needed to reach full scale on the A/D converters. The amplifier frequency response is wide enough to have negligible effect on the I & Q channel match.

Analog Devices HTC-0300 Track and Hold (T & H) Amplifier and HAS-1002 A/D converter were used for the I and Q quantizers. The A/D converter is a successive approximation type converter which requires that the input signal remain constant over the entire conversion interval in order to attain the rated 0.025 % of full scale accuracy (1/4 LSB); the T & H has been designed to work in conjunction with the HAS series converters to provide the required hold function. The T & H dynamic characteristics are the principal factors determining the quality of the quantized signal channel to channel match and dynamic range. The T & H has an aperture uncertainty of 100 picoseconds; at the maximum video signal bandwidth of 250 kHz, the T & H introduces a peak error of 0.016% (< 1/4 LSB of the converter) in the value of the signal voltage being sampled. The T & H has a droop rate of 0.005 millivolts per microsecond; over the 2.0 microsecond quantizing period, the output only changes by 0.01 millivolts, however. Since the LSB of the A/D converter is 7.32 millivolts, the T & H droop is a negligible factor in the quantizer operation. The T & H pedestal during the hold period is 5 millivolts. Since the pedestal is relatively insensitive to the voltage being held, it has the same effect as a DC bias and may, therefore, be cancelled out. The harmonic distortion level of

the T & H is 75 dB down making it a small contributor to the intermodulation products. The T & H also provides 60 dB of feed through rejection for signals up to ± 10 volts at the input.

There will also be small DC offset errors on the I and Q outputs of each receiver channel due to DC offset errors from the synchronous detector, the video amplifiers, the T & H and the A/D converter. Since the DC offsets were expected to be less than 3 LSBs of the A/D converter, only a small part of the A/D converter dynamic range is affected. DC bias correction feedback was not used, therefore, and DC offset corrections are accomplished in the digital corrections in the HP 9836 computer processing.

3.5.4 Recording and Control Subsystem. The Recording And Control Subsystem (RACS) interfaces the DBSA equipment and the HP 9836 computer used as the array beamformer, data display and antenna rotator controller. The RACS equipment includes a single board microprocessor which controls the data transfers between the computer and the array, translates computer control words to array configuration controls (frequency selection, calibration/data collection mode and test mode), performs local processing and controls a buffer memory. Figure 13 is a functional diagram for the RACS. The thirty-two serial digital outputs from the thirty-two receivers in the DBSA are transformed into parallel output before being stored in a buffer memory. The data interface has provisions for handling 12 bit I and Q data; only 10 bit A/D converters were used in the array, however.

During calibration of the array, the DBSA exciter is configured to generate a calibration pulse with a 125 kHz offset from the selected operational frequency and connect it to one side of the calibration feed. Each array calibration requires two sets of data to be collected; the first data set is taken with the calibration signal connected to the left side of the loop calibration feed. The second set of data is collected with calibration signal connected to the right side of the loop calibration feed. Two hundred and fifty six contiguous 10 bit I

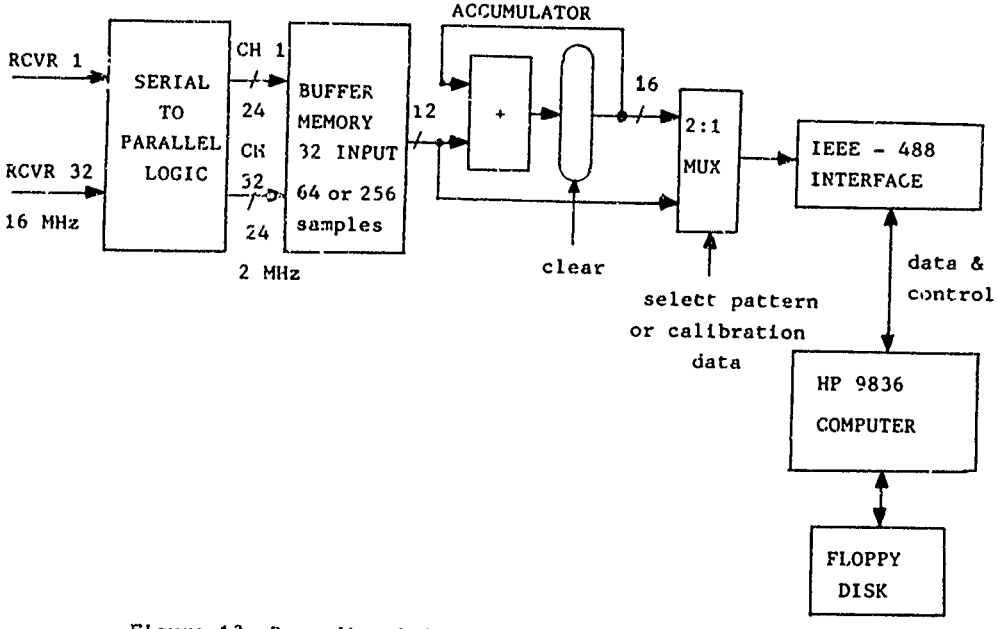

Figure 13. Recording & Control Subsystem Functional Diagram

and Q samples are collected from each of the 32 receivers and stored in the buffer memory for each data block. After each data block has been collected, the contents of the buffer memory is formatted into 8 bit bytes and transferred to the HP computer for calibration processing. The data is transferred over a standard IEEE-488 data interface at the rate determined by the HP interface controller.

Each block of 256 I and Q samples from a receiver (from the first set of calibration data) is processed to estimate the DC offsets in the I and Q samples and the amplitude balance and phase angle of the I and Q samples. The estimates of I and Q bias are used to correct the calibration data and all subsequent data that is collected. Similarly, the estimated correction coefficients to place the I and Q data in amplitude balance and phase quadrature are used to correct the calibration data and all subsequent data that is collected.

After the second calibration data block is collected and transferred to the HP computer, the data is normalized by the estimated DC offsets and I and Q balance corrections. The left side and right side data is than processed to estimate the insertion phase and gain differences between channels. At the completion of the processing on both sets of calibration data, correction coefficients are computed for the operating frequency that was used for calibration. The receiver correction coefficients are used to correct subsequent data from each receiver to remove DC bias errors, channel I and Q balance errors and channel to channel insertion phase and gain differences.

During pattern measurements, the RACS equipment disables the calibration test signal to permit data samples to be collected from the array using the source located in the far field of the array as the input signal. Blocks of 64 contiguous I and Q samples, from each receiver, are collected in the buffer memory as the array is rotating. At the end of each 64 sample block, the I and Q samples for each receiver are read out of the buffer by the RACS processor and separately accumulated (or equivalently coherently integrated) over 64 samples. The

integrated I and Q samples from the 32 receivers are transferred to the HP computer which reduces the data rate to the computer by a factor of 64 to 1; the signal to noise ratio of the pattern data is also increased by the signal integration performed in the RACS. The integrated I and Q data represents the array response at the angle the array face was during the data block collection. Since 64 samples are collected within 128 microseconds, the array may be considered to have not moved during the 64 samples.

Even with the 64 to 1 data compression prior to the computer, there is insufficient time to process the pattern data samples in the HP computer while the data is being collected. The pattern data samples from the RACS are saved in the computer until the array has rotated through the desired mechanical scan sector. Processing of the pattern data to normalize the data and to do digital beamforming is performed off line in non-real time.

3.5.5 Data processing software. The data processing software for the HP 9836 computer was written in HP Extended Basic 2.1 to permit it to be easily modified for future experiments and ease in integrating it with existing control software used to control the antenna rotator. The data processing software performs the following functions:

(1) Controls the DBSA array modes and operating frequency. Controls data transfers from the RACS subsystem to the HP9836.

(2) Provides an operator interface, via user menus, for specifying the DBSA equipment parameters, antenna rotator operating limits and pattern plotting parameters.

3) Controls calibration of the array and calculation of elemental receiver correction coefficients.

4) Controls collection of array pattern data and normalization of the array data.

5) Calculates array factor patterns with operator selectable Taylor amplitude weights for the data processed in the digital beamformer algorithm.

6) Displays and plots operator selected beam pattern data.

The receiver calibration to correct bias errors and I and Q errors makes use of an efficient DFT algorithm approach described by C. rchill, Ogar and Thompson in their paper[3]. The authors show that the use of a calibration frequency which is offset from the carrier frequency provides a means of estimating the I and Q amplitude balance and phase errors in terms of an image frequency which is present when there are amplitude balance and/or phase errors in the I and Q samples. The I and Q errors to be corrected are typically less than 5° degrees from phase quadrature and less than 1 dB from amplitude balance. With small errors, the primary response to the I and Q imbalance can be represented as producing an image of the offset frequency displaced in the opposite sense from the test signal that was generated. The power in the image response is approximately equal to 1/4 of the amplitude imbalance squared and 1/4 of the phase imbalance squared. The frequency offset on the calibration test signal permits the primary response and image responses to be separated by digital filters matched to the primary and image offsets.

The choice of a calibration frequency which has an offset equal to 1/4 of the data sampling rate results in a phase change of 90° from sample to sample for the offset frequency at the output of the synchronous detector. The digital filters to match the primary and image frequency degenerate to I and Q accumulators for each filter; the accumulators are preceded by an input selector that switches between the input I and Q samples and the negative of the I and Q components to provide filters with phase rotations of +90° and -90°. The offset frequency also provides a convenient means of measuring the DC offsets in the I and Q samples; a filter matched to DC will have zero output over contiguous sums of 4 samples in the I and Q

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[3]Churchill, F.E., Ogar, G.W., and Thompson, B. J., "The Correction of I and Q Errors in a Coherent Processor.", IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-17, No. 1, pp. 131-137, January 1981.

accumulators if the receiver channel has no DC offset. (The average value of any sine wave which has an even number of samples uniformly distributed over one cycle of the sine wave is equal to zero.)

The calibration correction coefficients for each receiver channel are estimated from processing 256 I and Q samples of the offset frequency calibration pulse collected over 512 microseconds of time; the unweighted digital filters have an approximate resolution of 2 kHz. The 125 kHz filter response (1/4 of sampling rate) has a null at DC and at -125 kHz which allows small DC offset errors and I and Q imbalances to be measured.

The errored I an Q samples from a receiver channel may be denoted by I_1 and Q_1, the signal may than be expressed as

$$I_1(t) = (1 + e)\ A \cos(W\ t) + a$$
$$Q_1(t) = A \sin(W\ t + D) + b$$

where
- e = the fractional amplitude imbalance
- D = the phase imbalance
- a = the DC offset in the I channel, and
- b = the DC offset ir the Q channel
- W = the offset frequency.

The DC offset errors are subtracted from the input signal prior to any other correction leaving unbiased I and Q signals which may be expressed as

$$I_2(t) = (1 + e)\ A \cos(W\ t)$$
$$Q_2(t) = A \sin(W\ t + D).$$

The I_2 and Q_2 signals are treated as vectors and two correction coefficients P and E are computed from the calibration data block. In matrix notation the signals after gain and phase correction designated as I_3 and Q_3 are related to I_2 and Q_2 as follows.

$$\begin{bmatrix} I_3 \\ Q_3 \end{bmatrix} = \begin{bmatrix} E & 0 \\ P & 1 \end{bmatrix} \begin{bmatrix} I_2 \\ Q_2 \end{bmatrix}$$

The signals I_3 and Q_3 are required to be orthogonal and equal in amplitude. The coefficients P and E are therefore related to the original errors as follows:

$$E = \cos(D) / (1 + e)$$
$$P = \sin(D) / (1 + e).$$

After application of the corrections, the signals are

$$I_3(t) = A \cos(D) \cos(W t)$$
$$Q_3(t) = A \cos(D) \sin(W t).$$

The corrected output signals for each receiver channel are scaled by the factor cos(D), the phase imbalance factor for the receiver. The correction factor has an impact on the channel to channel normalization corrections because it alters the gain of the channel. During the calibration measurements, the I and Q correction factors are applied to the receiver channel calibration data before the channels are compared; the gain factor change is, therefore, included in the channel correction factor.

The transfer function (insertion gain and phase) for a receiver channel is represented by a signal amplitude and phase value for the channel. This value is derived from the calibration signal measurements at the output of each receiver channel when the calibration signal source is connected to the left and right sides of the loop calibration feed as described in section 2.5.2. The two sets of calibration data, collected during each receiver measurement (data from feeding the left and right sides of the loop calibration feed), is corrected for DC bias and I and Q imbalance; the corrected data is integrated in a digital filter matched to the calibration offset frequency. The digital filter reduces the two sets of calibration data to a pair of I and Q samples representing the signal output from

feeding the left and right sides of the calibration feed. The complex square root of the product of the pair of I and Q samples is the signal amplitude and phase of the channel.

The first receiver channel is used as the reference channel. The insertion phase and gain of receiver channels 2 through 32 relative to receiver channel 1 is computed by dividing the signal amplitude and phase of channels 2 through 32 by the signal amplitude and phase of channel 1. A set of complex correction coefficients are computed (32) which are used to correct the pattern data from subsequent measurements.

During pattern measurements, 32 I and Q samples (one pair from each receiver) are stored, along with the antenna rotator mechanical pointing angle, each time the RACS subsystem transfers data to the computer. An I & Q pair is the sum of 64 samples from a DESA receiver. In the off-line play back of pattern data, each set of 32 I and Q stored pattern data samples is normalized by the last set of calibration coefficients recorded at the operating frequency used to collect the data. The normalization includes correction of the channel DC biases, correction of the channel I and Q amplitude and phase imbalances and finally correction of the channel insertion phase and insertion gain.

The 32 compensated and normalized receiver sample outputs from the 32 receiver channels are coherently combined by an FFT algorithm to produce the array factor response. The FFT algorithm is an efficient means of adding linear phase slopes to the receiver data and summing the receiver data. The 32 I and Q pairs may be amplitude weighted by one of the precomputed Taylor weight sets to suppress sidelobes. A 256 FFT point transform is performed on the weighted 32 I and Q samples to provide finer sampling of the array factor at intermediate phase slopes; the phase slopes are spaced in increments of 360/256 degrees from zero slope to 255 * 360/256 degrees per receiver. Array factor patterns are computed for each set of receiver I and Q samples over the rotator mechanical scan range.

The antenna response for one or more beam positions can be plotted against the array rotator position during play back of the array factor pattern data. The FFT output(s) corresponding to the desired electronic scan position(s) are plotted against the array rotator position to provide a conventional antenna pattern.

3.5.6 Mechanical implementation. The array elements, loop calibrator feed, receivers, exciter and clock control circuits are enclosed in a common weather tight enclosure. The array ground plane, Figure 14, is slotted to accept the strip line element arrays which are supported by a flange would bolts to the back side of the ground plane (Figure 9). A formed lexan cover over the array face provides weather protection for the dipoles; the cover is held in place and sealed by a clamping ring and gasket that seal the edges of the cover. The array element openings in the array ground plane are not weather tight; in addition, the dipoles can be shorted out if moisture accumulates in the slot area between the dipole arms at the tip of the dipoles (Figure 9). The dielectric constant of the lexan cover and its thickness distorts the array element patterns in the H plane at large scan angles; the cover must be removed for detailed pattern measurements.

The calibrator housing, shown in Figure 15, is a precision machined assembly. The loop feed strip line is recessed into a cavity machined in the cover. A thin metal sheet with non-directional coupling holes covers the loop feed to form a ground plane. The third machined part in the calibrator assembly provides cavities for the 32 receiver ports; the lower coupler strip line board is shown in place in one of the cavities and the upper and lower strip line boards is shown in the adjacent cavity. The lower coupler strip line board is shown in greater detail in Figure 16; the 20 dB directional coupler and the impedance matching fingers are in the lower part of the figure. An expanded area in the auxiliary arm corresponds to the region where the loop calibrator passes over

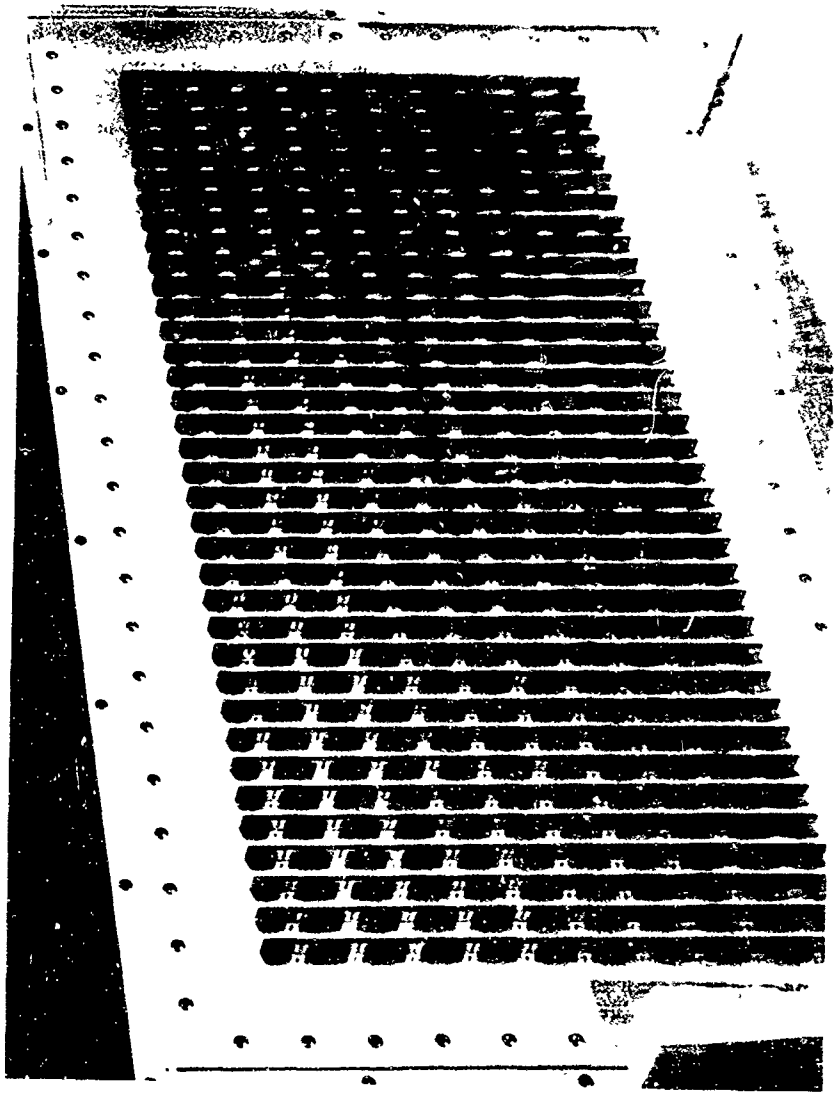


Figure 14. Array Ground Plane and Elements

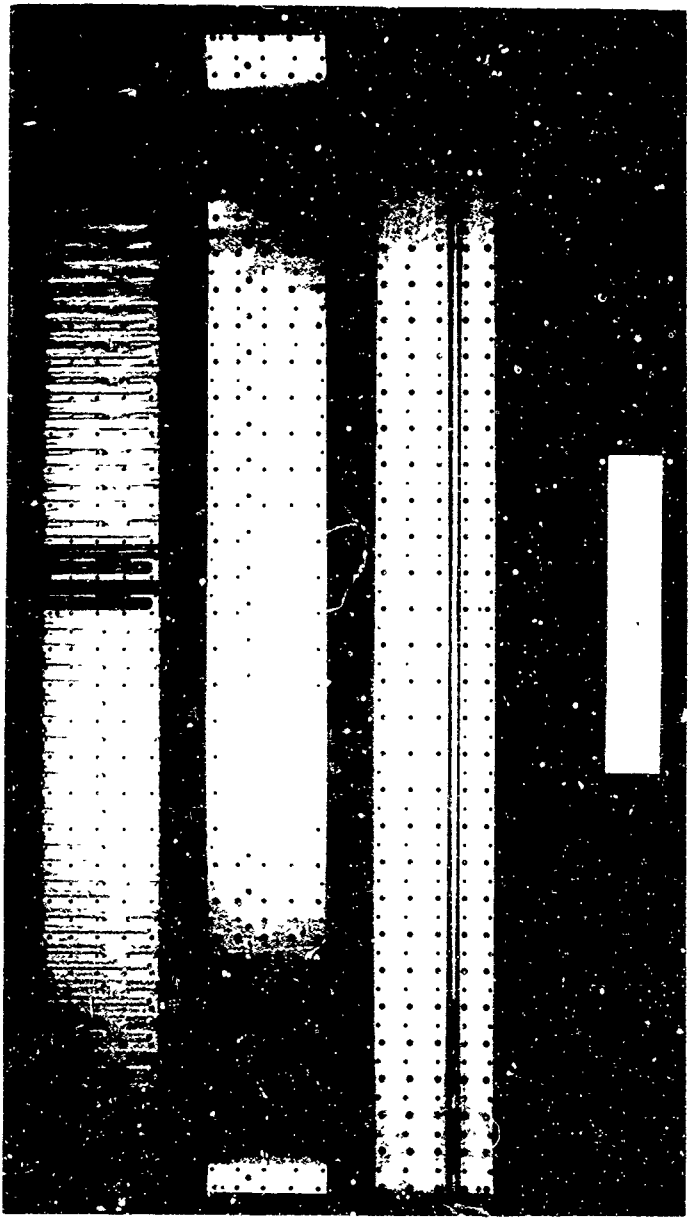


Figure 15. Calibrator Components

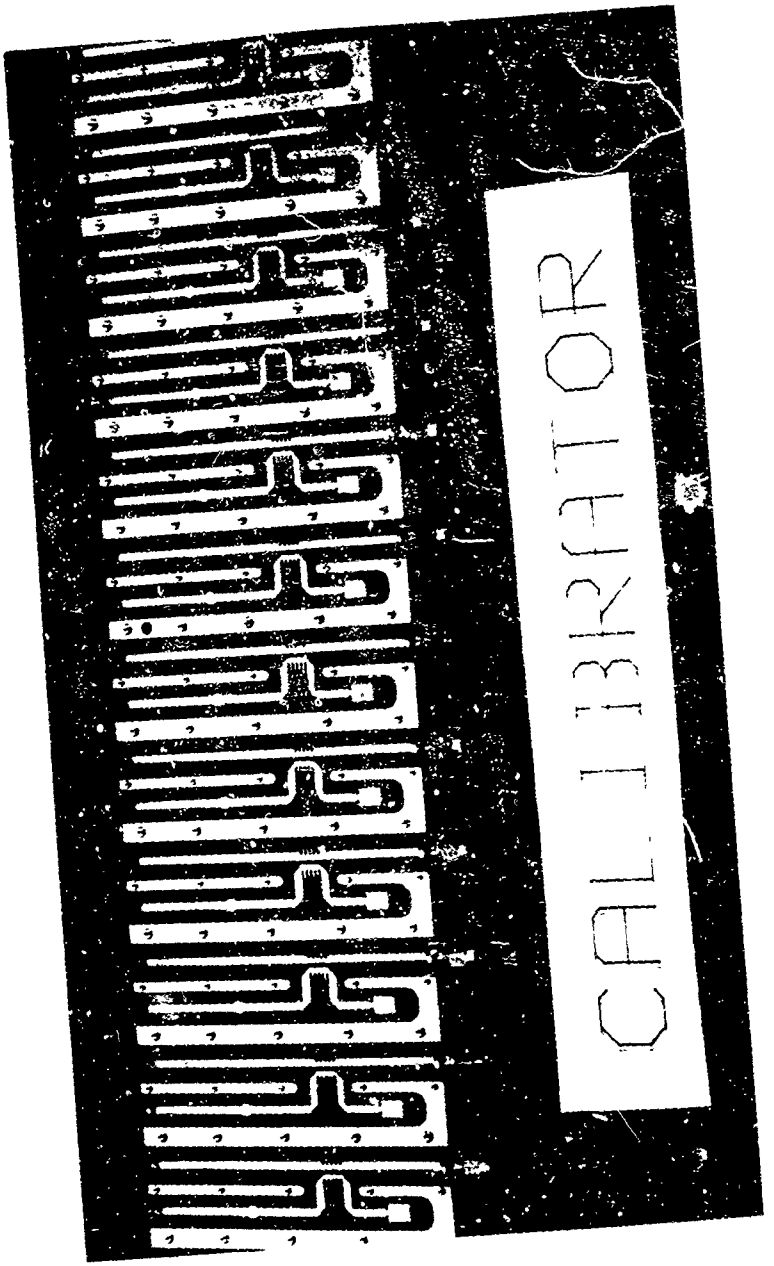


Figure 16. Calibrator Couplers

the receiver ports and the coupling hole is positioned in the ground plane. The assembled calibrator feed is shown mounted on the back side of the ground plane in Figure 17.

The elemental receivers were implemented with high performance commercially available components. The r-f amplifiers, mixers and filters are in separate packages with SMA connectors; the packaging isolates the individual receivers from each other (Figure 18). The i-f amplifier and balance of the receiver components are mounted on a two sided printed circuit board. The receivers were designed to be removed from the back side of the array (behind the ground plane); plunge type SMP connectors at the front end of the receiver provide the connections for the r-f input signal, the three LOs and a composite data clock for the Track and Hold, A/D converter and serial output shift register.

The exciter uses commercial phase locked synthesizers, commercially available amplifiers, a 5 MHz crystal clock and a custom times 14 multiplier. The power dividers for distributing the LOs and the reference frequency are implemented with commercial power dividers (Figure 19).

The DC power supplies to operate the array electronics are also housed in the antenna enclosure. Fans within the antenna enclosure provide cooling for all of the electronics, the air is directed past convection heat sinks at the top and bottom of the enclosure that transfer the heat load to the outside environment.

The RACS interface equipment was packaged separately and would be mounted near the HP 9836 computer to keep the IEEE interface cable length short. The transfer rate over the IEEE interface is limited by the length of the interface cable since data transfers involve handshaking between the two devices that are interfaced.

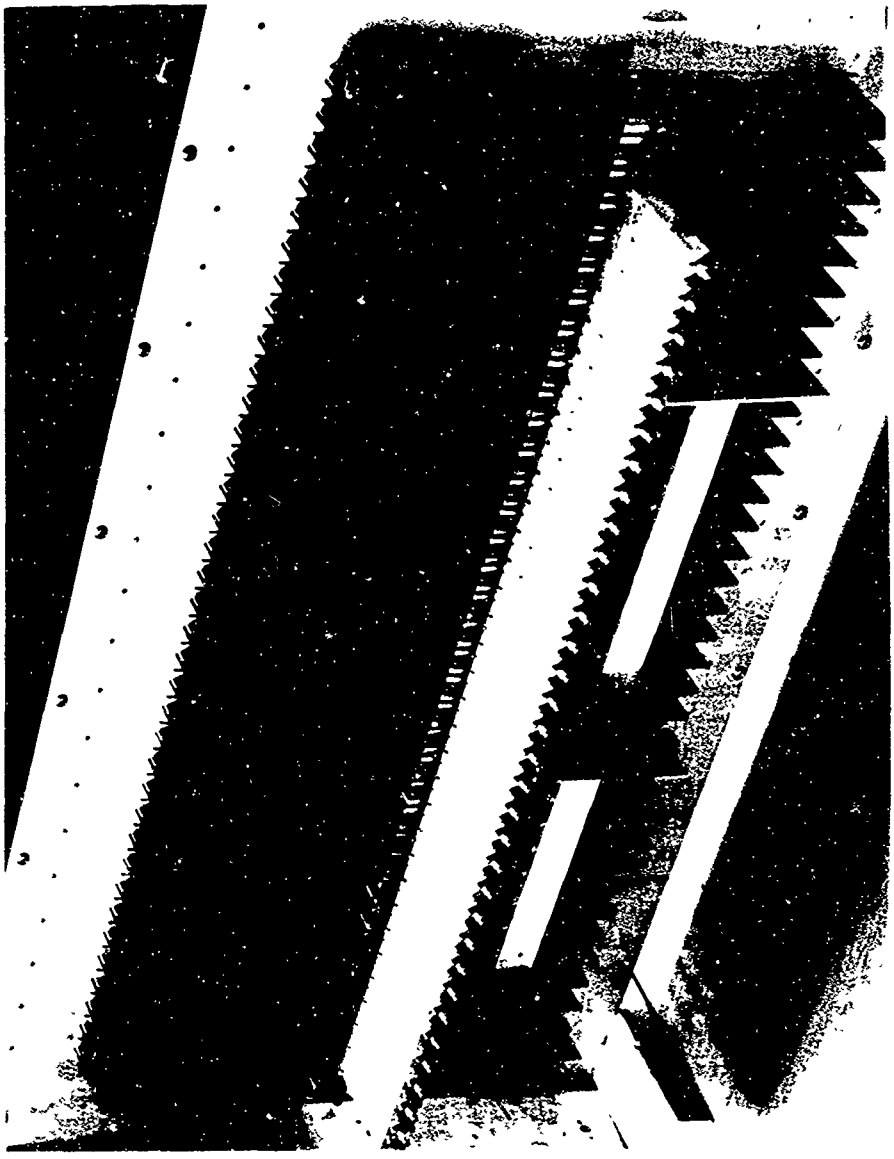


Figure 17. Calibration Feed and Element Radiation Interface

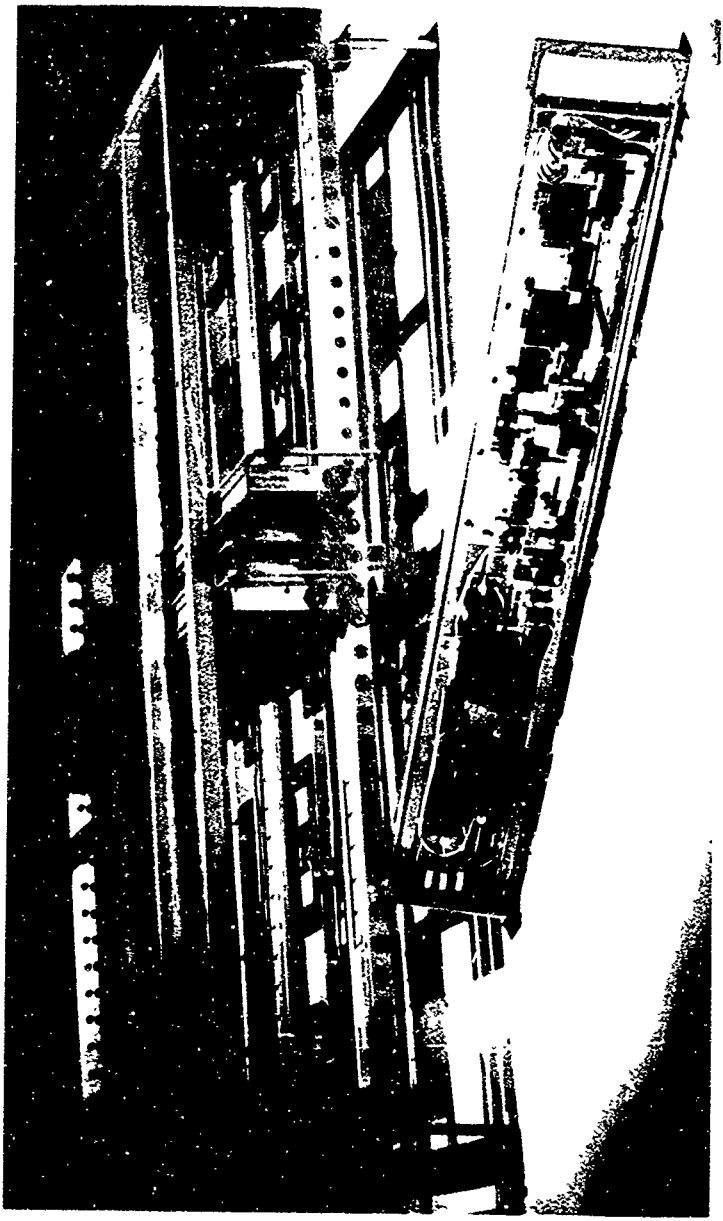


Figure 18. Receiver Rack Front View

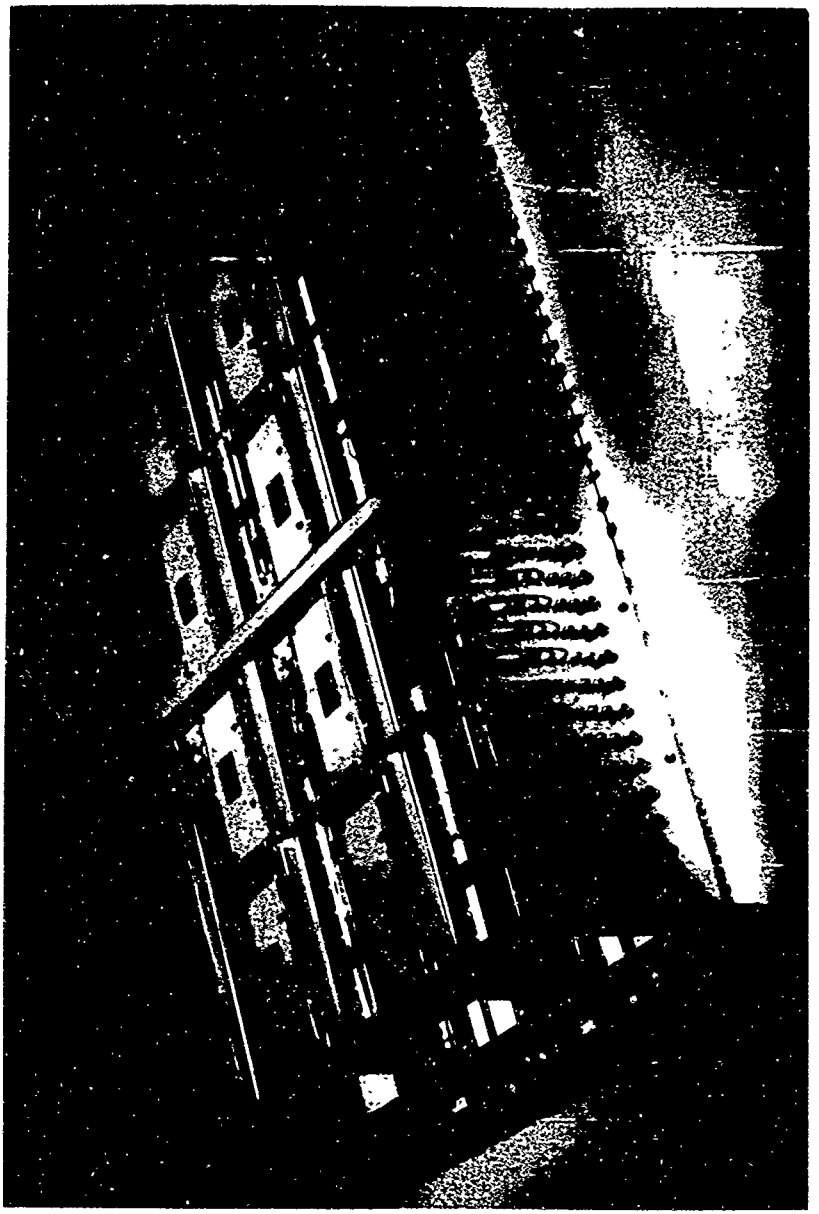


Figure 19. Receiver Rack Bottom View

SECTION 4
CONCLUSIONS

The preliminary assessment of the DBSA self-calibration approach indicates the measurement approach meets the objective of being able to compensate for construction variations in the receiver channels and changes in insertion phase and gain of the channels with temperature. The precision loop calibration feed, incorporated in the DBSA equipment, had low construction errors with low phase and amplitude errors. The loop calibrator approach, however, is limited by the correlated error introduced into the calibration measurements by small mismatches at the couplers and at the terminations on the load ends. In the present implementation form, the correlated error will also be present from row to row in a planar array; the correlated sidelobe will, therefore, not decrease as the array size is increased. (The remaining errors are, however, random and the average sidelobe level will decrease in a larger array.)

For arrays with very low peak and average sidelobe requirements, the corporate calibration feed will be required since correlated errors can be avoided in the distribution system. The corporate feed will, however, have to be calibrated in situ to obtain low measurement errors; it will also require periodic test to assure that accuracy of the system.

APPENDIX A

DERIVATION OF CHANNEL DECORRELATION FOR VARIOUS SYSTEM PARAMETERS

INTRODUCTION

In this appendix, derivations are given for equations that can be used to translate component phase, amplitude and timing errors into a correlation parameter. The correlation parameter defines the impact of the errors on the transfer function of the component; it is a measure of how identical the transfer functions are for two devices when both passing a wide band noise input signal. If the two channels (components) are identical, by definition their correlation coefficient is unity. If the channels are not identical the correlation coefficient will be less than one and imperfect cancellation will occur when the output of one channel is subtracted from the output of the second channel.

It can be shown that the maximum cancellation ratio is given by:

$$CR = (1 - |\rho|^2)^{-1}$$

The quantity $1 - |\rho|^2$ is referred to as the decorrelation. When there are multiple independent sources of mismatch, such as a string of filters and amplifiers, the composite correlation coefficient of the string is equal to the product of the correlation coefficients of each component itself.

Thus:

$$|\rho|^2 = |\rho_1|^2 \, |\rho_2|^2 \, \ldots\ldots \, |\rho_n|^2$$

1.0 DERIVATION OF CHANNEL DECORRELATION FOR VARIOUS SYSTEM PARAMETERS

This appendix derives the relationship between channel decorrelation, $1 - |\rho|^2$, and the following system parameters:

1) Amplitude and Phase Mismatch Between Receivers
2) Sampling Jitter
3) I/Q Balance and Orthogonality
4) Receiver Time Delay Mismatch

1.1 Amplitude and Phase Mismatch

Amplitude and phase mismatch of the transfer functions of two channels are important sources of decorrelation. The amount of decorrelation can be related to the weighted mean square difference in amplitude and phase. To show this, let the transfer functions of two nearly identical channels be $G_1(f)$ and $G_2(f)$ and express their ratio as:

$$\frac{G_2(f)}{G_1(f)} = \mu \exp [\alpha (f) + j \, \phi (f)] \qquad \text{(A-1)}$$

where:

μ = a complex constant

$\exp \alpha (f)$ = the amplitude ratio function

$\phi (f)$ = the phase difference function

Both α and ϕ are assumed to be very small and the constant μ is chosen so that the weighted mean values of α and ϕ are zero; that is,

$$\int G_1(f)^2 \, \alpha \, (f) \, df = 0 \tag{A-2}$$

$$\int G_1(f)^2 \, \phi \, (f) \, df = 0 \tag{A-3}$$

The weighted mean square values (variances) of α and ϕ are defined as:

$$\sigma_\alpha^2 = \int |G_1(f)|^2 \; \alpha^2(f) \, df \tag{A-4}$$

$$\sigma_\phi^2 = \int |G_1(f)|^2 \; \phi^2(f) \, df \tag{A-5}$$

If it is also assumed that α and ϕ are "uncorrelated" in the sense that:

$$\int |G1(f)|^2 \, \alpha \, (f) \, \phi \, (f) \, df = 0 \tag{A-6}$$

then we can show that the decorrelation,

$$1 - |\rho|^2 = \sigma_\alpha^2 + \sigma_\phi^2 \qquad \text{(A-7)}$$

Table A-1 gives the values of τ_ϕ in degrees and $(1 + \sigma_\alpha)$ in dB required to achieve the decorrelation given in the first column. It is assumed here that the decorrelation is equally divided between phase and amplitude ($\sigma_\alpha = \sigma_\phi$ with σ_ϕ in radians). Note that for small σ_α, the amplitude entries may be calculated as:

$$20 \log_{10} (1 + \sigma_\alpha) = 8.686\ \sigma_\alpha \qquad \text{(A-8)}$$

1.2 Sampling Jitter

Another source of decorrelation is sampling time jitter in the sample and hold function of the A/D converters. A constant difference of τ seconds in the sampling times of two otherwise identical channels would result in a cross-correlation coefficient of:

$$\rho(\tau) = \frac{R(\tau)}{R(0)} \qquad \text{(A-9)}$$

where $R(\tau)$ is the autocorrelation of the output of either channel with white noise input.

Table A-1

Amplitude and Phase Match

$$\frac{G_a(f)}{G_b(f)} = \exp\left[\alpha(f) + j\,\phi(f)\right]$$

$$1 - |\rho|^2 = \sigma_\alpha^2 + \sigma_\phi^2$$

$1 - \lvert\rho\rvert^2$ (dB)	$1 + \sigma_\alpha$ (dB)	σ_ϕ (deg)
-20	.593	4.051
-30	.192	1.281
-40	.061	.405
-50	.019	.128
-60	.006	.041

If the channel frequency response characteristics are rectangular in amplitude with two-sided bandwidth β, and with linear phase, the correlation coefficient will be

$$\rho(\tau) = \frac{\sin \pi \beta\tau}{\pi \beta\tau} \tag{A-10}$$

For small τ, the decorrelation in this case may be approximated by

$$1 - |\rho|^2 \simeq \left(\frac{\pi \beta\tau}{3}\right)^2 \tag{A-11}$$

For a Gaussian-shaped transfer function with 3 dB bandwidth of β, we have:

$$\rho(\tau) = \exp\left\{-\frac{(\pi \beta\tau)^2}{4 \ln 2}\right\} \tag{A-12}$$

and for small τ in this case,

$$1 - |\rho|^2 \simeq \frac{(\pi \beta\tau)^2}{2 \ln 2} \tag{A-13}$$

To obtain the decorrelation with time jitter, Equations (A-11) and (A-13) must be averaged with respect to τ. Assuming a uniform distribution of sampling time jitter over the interval (-T, T) in both channels, the average value of τ^2 is found to be

$$\bar{\tau}^2 = \frac{1}{4T^2} \int_{-T}^{T} \int_{-T}^{T} (t_1 + t_2)^2 \, d t_1 \, d t_2 \qquad \text{(A-14)}$$

Assuming the jitter in each channel is independent, this simplifies to

$$\bar{\tau}^2 = \frac{1}{T} \int_{-\tau}^{\tau} t^2 \, d t \qquad \text{(A-15)}$$

$$= \frac{2T^2}{3} \qquad \text{(A-16)}$$

With this value, we obtain for the rectangular frequency response characteristic

$$1 - |\rho|^2 \doteq 2/9 \, (\pi \beta T)^2 \qquad \text{(A-17)}$$

and for the Gaussian frequency response characteristic,

$$1 - |\rho|^2 \doteq \frac{(\pi \beta T)^2}{3 \ln 2} \qquad \text{(A-18)}$$

Values of $1 - |\rho|^2$ for the rectangular frequency response characteristic are tabulated for three different bandwidths in Table A-2. The sampling jitter is expected to be held to 25 ps for which the decorrelation is -68.63 dB with a 10 MHz bandwidth.

Table A-2

Sampling Jitter Decorrelation

Jitter	$1 \|\rho\|^2$ (dB)		
T(ps)	1 MHz	5 MHz	10 MHz
5	-102.61	-88.63	-82.61
10	-96.59	-82.61	-76.59
15	-93.07	-79.09	-73.07
20	-90.57	-76.59	-70.57
25	-88.63	-74.65	-68.63
50	-82.61	-68.63	-62.61
75	-79.09	-65.11	-59.09
100	-76.59	-62.61	-56.59

1.3 I/Q Balance and Orthogonality

The baseband I&Q components of each channel are formed in synchronous detectors that multiply the IF input signal by nominally equal amplitude local sinusoids 90° apart in phase. Any unbalance in amplitude or deviation from orthogonality will cause channel-to-channel

decorrelation. The decorrelation is derived as follows:

Represent the I&Q components by:

$$I = \mathrm{Re}\,(a \exp j\,\alpha)\, v \tag{A-19}$$

$$Q = \mathrm{Im}\,(b \exp j\,\beta)\, v \tag{A-20}$$

Here, "v" is the complex envelope of the IF input to the synchronous detector "a", and "b" are the amplitudes associated with the respective channels, and "α" and "β" the phase deviations from their nominal reference values. Ideally, we should have $a = b$ and $\alpha = \beta$.

The real and imaginary part of v are denoted as I_o and Q_o; that is,

$$v = I_o + jQ_o \tag{A-21}$$

where

$$E\,(|I_o|^2) = E\,(|Q_o|^2) = P \tag{A-22}$$

and

$$E\,(I_o\, Q_o^*) = 0 \tag{A-23}$$

With this notation, Equations (A-19) and (A-20) become

$$I = a\,(I_o \cos\alpha - Q_o \sin\alpha) \tag{A-24}$$

$$Q = b\,(I_o \sin\beta - Q_o \cos\beta) \tag{A-25}$$

The covariance of the output of the errored channel with a perfect channel $(I_o + jQ_o)$, is

$$\mu = E\,[(I + jQ)\,(I_o - jQ_o)] \tag{A-26}$$

$$\mu = E\,[(I\,I_o + Q\,Q_o) + j\,(Q\,I_o - I\,Q_o)] \tag{A-27}$$

Using Equations (A-22) through (A-25) we find

$$E\,(I\,I_o) = a\,P\cos\alpha \tag{A-28}$$

$$E\,(Q\,Q_o) = b\,P\cos\beta \tag{A-29}$$

$$E\,(Q\,I_o) = b\,P\sin\beta \tag{A-30}$$

$$E\,(I\,Q_o) = a\,P\,.in\,\alpha \tag{A-31}$$

Substituting these quantities in Equation (A-27), we obtain

$$u = P\,[a \exp(-j\,\alpha) + b \exp(j\,\beta)] \tag{A-32}$$

The correlation coefficient magnitude squared is, therefore,

$$|\rho|^2 = \frac{|M|^2}{(I^2 + Q^2)\,(I_o^2 + Q_o^2)} \tag{A-33}$$

$$= \frac{|u|^2}{2P^2\,(a^2 + b^2)} \tag{A-34}$$

$$= \frac{a^2 + b^2 + 2\,a\,b\cos(\alpha - \beta)}{2\,(a^2 + b^2)} \tag{A-35}$$

and the decorrelation is

$$1 - |\rho|^2 = \frac{a^2 + b^2 - 2\,a\,b\cos(\alpha - \beta)}{2\,(a^2 + b^2)} \qquad \text{(A-36)}$$

$$= \frac{(a - b)^2 - 2\,a\,b\,[1 - \cos(\alpha - \beta)]}{} \qquad \text{(A-37)}$$

Assuming $(a - b)$ and $(\alpha - \beta)$ are very small, and using the notation

$$\delta a = a - b$$
$$\delta \phi = \alpha - \beta$$

we get

$$1 - |\rho|^2 = 1/4 \left\{ \left(\frac{\delta a}{a}\right)^2 + \delta \phi^2 \right\} \qquad \text{(A-38)}$$

Since $\delta \alpha$ and $\delta \phi$ will vary from channel-to-channel and with time we should use average values. Furthermore, since Equation (A-38) gives the decorrelation between an errored channel and an unerrored channel, the decorrelation between two errored channels will be doubled. Our final result, therefore, is

$$1 - |\rho|^2 = 1/2 \left\{ \left(\frac{\overline{\delta a}}{a} \right)^2 + \overline{\delta \phi^2} \right\} \qquad \text{(A-39)}$$

Table A-3 was constructed using this formula. It gives the amount of amplitude unbalance and phase deviation corresponding to different amounts of decorrelation assuming both contribute equally.

Table A-3

I/Q Balance and Orthogonality

$1 - \|\rho\|^2$ (dB)	$1 + \delta a/a$ (dB)	$\delta\phi$ (deg)
-20	.828	5.730
-30	.220	1.812
-40	.086	.573
-44.5	.050	.350
-50	.027	.181
-60	.0087	.0573

2.0 DYNAMIC RANGE EFFECTS ON CANCELLATION RATIO

This appendix derives the relationships between the cancellation ratio and the following system parameters:

1. Receiver Third Order Intercept Point
2. A/D Quantization and Threshold Noise
3. A/D Full Scale Input Voltage (saturation effects)

2.1 Third Order Intercept Point

The dynamic range requirements of the analog portion of each channel, from the antenna to the A/D converter, may be expressed in terms of the "third order intercept point".

Let the transfer characteristic of the analog portion of the channel be represented by the polynomial.

$$e = k\ (v + \alpha\ v^3) \qquad \text{(A-40)}$$

where v is the input, e the output, and k and α are constants. Even order terms give rise to out-of-band components that are removed by a zonal filter and so are omitted. The input v is assumed to be sufficiently small that the fifth and higher order terms may be neglected.

Now let the input be the sinusoid

$$v(t) = a \cos \omega t \tag{A-41}$$

with power,

$$p = 1/2\ a^2 \tag{A-42}$$

then

$$e = \{(a \cos \omega t + \alpha\ a^3 \cos^3 \omega t)\} \tag{A-43}$$

Expanding the cubic term and retaining only the fundamental, gives

$$e = k\ (a + 3/4\ \alpha\ a^3) \cos \omega t \tag{A-44}$$

Incidental phase modulation is not explicitly shown in this representation. If it were present, it would be associated with the cubic term and would not affect the results obtained here.

The output power in the linear and cubic terms of Equation (A-44) are

$$P_1 = k^2\ p \tag{A-45}$$

and

$$P_3 = k^2\ 9/4\ \alpha^2\ p^3 \tag{A-46}$$

By definition, the third order intercept point occurs at the level of input power, P_i, for which the output powers are equal; i.e., $P_3 = P_1$ or where

$$k^2\ \frac{9\alpha^2}{4}\ P_i^3 = k^2\ P_i \tag{A-47}$$

from which we get

$$P_i = \frac{2}{3\alpha} \tag{A-48}$$

Substituting for α in Equation (A-46) gives

$$P_3 = k^2\ \frac{P^3}{P_i^2} \tag{A-49}$$

The linear term in Equation (A-44) will be adaptively cancelled leaving the cubic term as a residue. To evaluate the residue we assume the input jamming has a bivariate Gaussian probability density function. The instantaneous input power will, therefore, have the exponential PDF

$$f(p) = \frac{1}{\mu} e^{-p/\mu} \tag{A-50}$$

where μ = average power of the jamming. The average cubic residue power will, therefore, be

$$\overline{p_3} = \frac{k^2}{p_1^2} \int_0^\infty p^3 \frac{1}{\mu} e^{-p/\mu} \, dp \tag{A-51}$$

$$= \frac{k^2}{p_1^2} 6 \mu^3$$

The average output power of the linear term will be

$$\overline{p_1} = k^2 \int_0^\infty p \frac{1}{\mu} e^{-p/\mu} \, dp = k^2 \mu \tag{A-52}$$

Taking the ratio of $\overline{p_1}$ to $\overline{p_3}$, we obtain the cancellation ratio limit (CRL) imposed by the cubic non-linearity,

$$1/6\left(\frac{p_1}{\mu}\right)^2$$

$$= 2\left(\frac{p_1}{\mu}\right)_{dB} - 7.782 \text{ dB} \qquad \text{(A-53)}$$

This formula is tabulated in Table A-5.

Table A-5

Cancellation Ratio Limit

$\left(\frac{p_1}{\mu}\right)$ dB	CRL dB
15	22.22
20	32.22
25	42.22
30	52.22
35	62.22
40	72.22

The 30 dB level is a reasonable goal to set for the ratio of the third order intercept point to the average input power. For a JNR of 50 dB this implies a dynamic range of 80 dB measured from the noise level to the third order intercept point. From Table 2-1 we noted that the 30 dB level corresponds to a CRL of 52.22 dB.

2.2 A/D Quantization and Threshold Noise

If the A/D threshold levels are uniformly spaced over the range of the A/D converter, the quantization intervals will be constant and the quantization noise will be $q^2/12$ where q is the length of the interval. However, random variations in the threshold levels will produce random variations in the lengths of the intervals. The quantization noise is obtained by averaging over the quantization intervals.

Let λ be the length of a random interval and assume that the PDF of λ is

$$p(\lambda) = \begin{cases} \lambda/a, & (1-d)\ q \le \lambda \le (1+d)\ q \\ 0 & \text{elsewhere} \end{cases} \qquad \text{(A-54)}$$

Here, "q" is the average interval length, d is a parameter, and

$$a = \int_{(1-d)\,q}^{(1+d)\,q} \lambda\, d\lambda = 2\, d\, q^2 \qquad \text{(A-55)}$$

The average quantization noise will be

$$\sigma_q^2 = \int_{(1-d)\,q}^{(1+d)\,q} \frac{\lambda^2}{12}\, p(\lambda)\, d\lambda \qquad (A\text{-}56)$$

$$= \frac{q^2}{12}(1 + d^2)$$

Many manufacturers specify a tolerance of $\pm 1/2$ interval on the threshold levels. This corresponds to $d = 1/2$ for which we obtain

$$\sigma_q = 5/4\, \frac{q^2}{12} = \frac{5}{48}\, q^2 \qquad (A\text{-}57)$$

If σ_n^2 is the system noise level and σ_n/q is 1, then

$$\frac{\sigma_q^2 + \sigma_n^2}{\sigma_n^2} = 1 + \left(\frac{\sigma_q}{q}\right)^2 = 1 + 5/48 = 0.43\ \text{dB} \qquad (A\text{-}58)$$

There may also be a systematic variation in the threshold levels of the A/D converter. For example, the quantization intervals may be smaller for low inputs than for high inputs. This is equivalent to a non-linear input-output transfer characteristic and can be analyzed as

an analog non-linear distortion.

Consider an A/D converter with cubic distortion in its transfer characteristic g(x), where

$$g(x) = x + \alpha x \left[1 - \left(\frac{x}{V_m}\right)^2\right] \quad -V_n \leq x \leq V_m \tag{A-59}$$

where x is the input voltage, $2V_m$ is the input voltage range, and parameter. We define α in terms of the maximum deviation of g(x) from a linear characteristic. The deviation at any input x is

$$D(x) = \alpha x \left[1 - \left(\frac{x}{V_m}\right)^2\right] \tag{A-60}$$

and the maximum deviation occurs where

$$\frac{dD}{dx} = 0 = \alpha \left[1 - 3\left(\frac{x}{V_m}\right)^2\right] \tag{A-61}$$

or at

$$x = \hat{x} = \frac{V_m}{\sqrt{3}} \tag{A-62}$$

The maximum deviation is

$$D(\hat{x}) = \delta = \frac{2\alpha}{3\sqrt{3}} V_m \tag{A-63}$$

For an N-bit A/D converter with average quantization interval, q, we have,

$$V_m = 2^{N-1} q \tag{A-64}$$

so that

$$\delta = \frac{2^N \alpha q}{3\sqrt{3}} \tag{A-65}$$

Next, we find the power in the deviation or distortion term. This will be residue under the assumption that the linear term is cancelled. We assume the input is Gaussian with mean zero and sigma ψ. Then

$$\overline{D^2} = \int_{-V_m}^{V_m} D^2(x) \frac{1}{\sqrt{2\pi}\,\psi} \exp\left(-x^2/2\psi^2\right) dx \tag{A-66}$$

Using Equation (A-60) FOR D(x), replacing the integral limits by $\pm$ infinity to obtain an upper bound, and using Equation (A-65) to replace α, we get

$$\overline{D^2} \leq \frac{27}{2^{2N}} (\delta/q)^2 \mu (1-6 \mu + 15 \mu^2) \qquad \text{(A-67)}$$

where

$$\mu = \left(\frac{\psi}{V_m}\right)^2 \qquad \text{(A-68)}$$

In the next section, we show that the average input power should be about 15 dB below the saturation level of the A/D converter, V_m^2, to ensure that saturation effects do not limit cancellation below 60 dB. With μ = .0316 (-15 dB) in Equation (A-67), we obtain

$$\overline{D^2} \leq \frac{27}{2^{2N}} (0.0261) \left(\frac{\delta}{q}\right)^2 \qquad \text{(A-69)}$$

or

$$\overline{D^2} \leq (20 \log \frac{\delta}{q} - 6.02 N - 1.52) \text{ dB} \qquad \text{(A-70)}$$

For N = 12, this becomes

$$\overline{D^2} \leq (20 \log \frac{\delta}{q} - 73.77) \text{ dB} \qquad \text{(A-71)}$$

From this, we conclude that if δ is less than 5 q, cancellation will not be affected at the -60 dB level. The low value of μ, incidently, implies that $\overline{D^2}$ will be very close to the upper bound given by Equation (A-70).

2.3 A/D Saturation

A/D converters operate over a limited input voltage range, from say $-V_m$ to $+V_m$. When these limits are ex- ceeded, in either direction, the input in effect saturates at the peak level. The limits will always be exceeded with noise jamming at a rate that depends upon the average jamming power.

When saturation occurs, the cancellation balance is upset and the residue may increase by as much as the difference between the true voltage and the saturation level. The power in this difference is referred to here as the overflow power. Assuming a Gaussian distribution for the I and Q components, with power equal to σ^2, the overflow in the I or Q channels will be

$$\text{Overflow Power} = \frac{2}{\sqrt{2\pi}\,\sigma} \int_{V_m}^{\infty} (V-V_m)^2 \, e^{-V^2/2\sigma^2} \, dV \qquad \text{(A-72)}$$

The ratio of this power to the input power, σ^2, may be written as

$$\frac{\text{Overflow Power}}{\sigma^2} = \sqrt{\frac{2}{\pi}} \int_L^\infty (X-L)^2 \, e^{-x^2/2} \, dx \qquad \text{(A-73)}$$

where

$$L = \frac{V_m}{\sigma} \qquad \text{(A-74)}$$

The overflow power ratio is tabulated in Table A-6 as a function of L.

Table A-6

Overflow Power

L (dB)	Overflow Power/σ^2(dB)
10.0	-35.4
10.2	-36.7
10.4	-37.9
10.6	-39.3
10.8	-40.6
11.0	-42.1
11.2	-43.6
11.4	-45.1
11.6	-46.7
11.8	-48.4
12.0	-50.2
12.2	-52.8
12.4	-53.9
12.6	-55.9
12.8	-58.0
13.0	-60.2
13.2	-62.4
13.4	-64.8
13.6	-67.2
13.8	-69.8
14.0	-72.5
14.2	-75.2
14.4	-78.2
14.6	-81.2
14.8	-84.4
15.0	-87.7

It may be seen that the overflow power ratio varies quite rapidly with L and is almost -70 dB when L, the ratio of the maximum A/D voltage to the RMS input, is 14 dB or greater. At -70 dB, the effect on the attainable cancellation is negligible.

2.4 Word Size and Dynamic Range

The dynamic range of the A/D converter is defined here as the maximum JNR (jammer-to-noise ratio) that can be obtained allowing 15 dB of margin for overflow. The quantization interval, q, is a function of the voltage range, 2 V_m, and the number of bits. With N bits there are 2^N quantization intervals with average length,

$$q = \frac{2\ V_m}{2^N} \tag{A-75}$$

Hence,

$$\frac{V_m}{q} = 2^{N-1} \tag{A-76}$$

Let the input system noise be denoted by $\sigma_n 2$ and the maximum instantaneous power level that can be converted by P_{max}. Then

$$P_{max} = V_m^{\ 2} \tag{A-77}$$

and

$$\frac{P_{max}}{\sigma_n^2} = \frac{V_m^2}{(\sigma_n/q)^2 q^2} = \frac{2^2 (n-1)}{(\sigma_n/q)^2} \tag{A-78}$$

$$= [6.02 (N-1) - 20 \log \left(\frac{\sigma_n}{q}\right)] \text{ dB} \tag{A-79}$$

For $\frac{\sigma_n}{q} = 1$ and $N = 12$, Equation (A-79) yields

$$\frac{P_{max}}{\sigma_n^2} = 66.23 \text{ dB} \tag{A-80}$$

To get the dynamic range we must subtract from this .43 dB for quantization and threshold noise and 15 dB for overflow margin. This gives:

$$\text{A/D dynamic range} = 50.80 \text{ dB} \tag{A-81}$$

APPENDIX B
LOOP CALIBRATOR

The loop calibration concept for DBSA was described in Section 2. In this appendix, the error sources in the calibrator are considered along with the impact of the errors on the array patterns.

The analysis of the calibration TL (transmission line) loop is shown in Figure B-1. The circuit conditions for the two switch settings are shown in Figures B-1a and B-1b. The analysis utilizes S-parameters, e.g., the "A" network is characterized by A_{11}, A_{21}, A_{12} and A_{22}, and all the source and load resistances are normalized to unity. For reciprocal networks $A_{12} = A_{21}$. The calibration generator is matched and sends out incident voltages $V_{inc\ 1}$ and $V_{inc\ 2}$. The load end calibration voltages are $V_{cal\ 1}$ and $V_{cal\ 2}$.

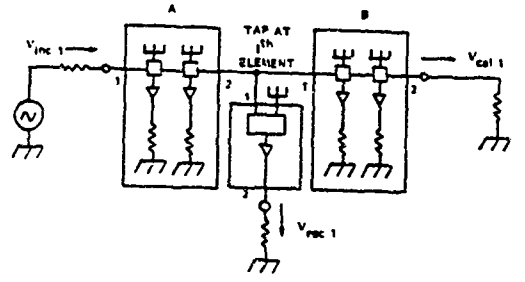
The tap is art the i^{th} position, i.e., networks "A" and "B" represent all the transmission lines and taps to the left and right of this tap, respectively. Figure B-2a illustrates that the voltage reflection coefficients looking to the left and right of the i^{th} tap are A_{22} and B_{11}, respectively, in the calibration loop. The i^{th} tap calibration network, antenna, and receiver string are represented by a normalized shunt admittance y on the calibration loop as shown in Figure B-2b. (The normalized admittance y is equal to Y/Y_o, where $Y_o = 1/Z_o$ and Z_o is the TL characteristic impedance.) The total loop network is "T" and is composed of A, D, and B. (Networks T, A, and B are represented by S-parameters T, A, and B, respectively.) The i^{th} tap voltage across the tap admittance is $V_{tap\ 1}$ and $V_{tap\ 2}$.

Referring to Figures B-1 and B-2, the two received loop calibration voltages are

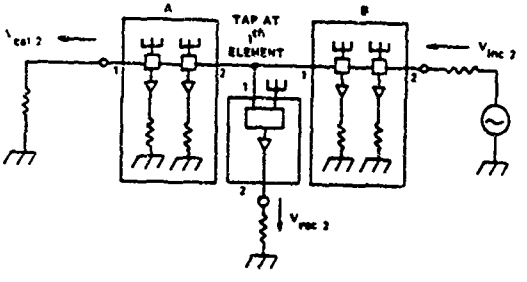
$$V_{cal\ 1} = T_{21}\ V_{inc\ 1} \qquad \text{(B-1a)}$$

and

$$V_{cal\ 2} = T_{12}\ V_{inc\ 2} \qquad \text{(B-1b)}$$



a) CALIBRATION SWITCH IN POSITION #1



b) CALIBRATION SWITCH IN POSITION #2

Figure B-1. Calibration Loop for Both Switch Positions

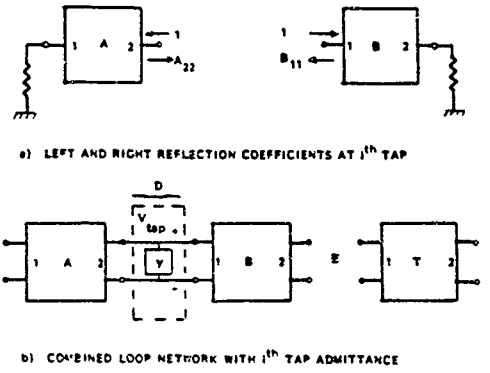


Figure B-2. Block Diagram of Calibration Loop

From an S-parameter analysis, the two tap voltages at the i^{th} tap are

$$V_{tap\ 1} = [A_{21}(1 + B_{11})(1 + D_{11})/(1 - E)]\ V_{inc\ 1} \qquad (B\text{-}2a)$$

$$V_{tap\ 2} = [B_{12}(1 + A_{22})(1 + D_{11})/(1 - E)]\ V_{inc\ 2} \qquad (B\text{-}2b)$$

where $E = A_{22}B_{11} + D_{11}(A_{22} + B_{11} + 2\ A_{22}\ B_{11})$ (B-3)

(and is composed of second order or higher terms due to multiple reflections). The reflecxtion coefficient for the tap shunt admittance y is

$$D_{11} = -y/(2 + y) = D_{22} \qquad (B\text{-}4a)$$

and the transmission across the admittance is

$$D_{21} = 1 + D_{11} = 2/(2 + y) = D_{12} \qquad (B\text{-}4b)$$

Note that the calibration loop contains only reciprocal networks, i.e.,

$$A_{12} = A_{21} \qquad (B\text{-}5a)$$

$$B_{12} = B_{21} \qquad (B\text{-}5b)$$

$$T_{12} = T_{21} \qquad (B\text{-}5c)$$

and that the total loop transmission S-parameter is

$$T_{21} = \frac{A_{21}\ B_{21}(1 + D_{11})}{(1 - E)} \qquad (B\text{-}6)$$

The product of the two tap voltages at the i^{th} tap is

$$V_{tap\ 1}\ V_{tap\ 2} = \frac{T_{21}(1 + D_{11})(1 + A_{22})(1 + B_{11})\ V_{inc\ 1}\ V_{inc\ 2}}{(1 - E)} \qquad (B\text{-}7)$$

The effective calibration voltage

$$V^i = \mathrm{Sqrt}(V^i_{tap\ 1}\ V^i_{tap\ 2}) \qquad (B\text{-}8)$$

is obtained from two sets of simultaneous measurements of all tap voltages (or equivalently, the transmission coefficients) when fed from the left ($V_{tap\ 1}$) and from the right ($V_{tap\ 2}$). Ideally, all voltages V^i would have identical amplitudes and phases which would be the case if the shunt coupling elements

were identical and the reflection seen from each tap were the same or zero.

When the effects of mismatch at the ends of the loop are included, the expression for the product of tap voltages becomes

$$V_{tap\ 1}V_{tap\ 2} = V_{inc\ 1}\,V_{inc\ 2}\,\frac{T_{21}(1 + D_{11})}{(1 - E)}\,\frac{[(1 + A_{22})(1 - R_L A_{11}) + R_L A_{12}A_{21}]}{[(1 + B_{11})(1 - R_R B_{22}) + R_R B_{12}B_{21}]} \qquad \text{(B-9)}$$

where

R_L and R_R are the reflection coefficients for the terminations on the left and right sides of the loop respectively and the S-parameters are the same as previcusly defined.

A test model for the non-directional coupler was built and tested on an IR&D study. The model consisted of two 50 ohm transmission lines with one crossing over the other. The transmission lines couple at their intersection through a 0.150 inch diameter hole which produces - 35 dB coupling in each direction to the coupled line. An equivalent circuit for the coupling tap is shown in Figure B-3.

The value of C_s represents the mismatch at the junction the actual value depends on the matching circuit on the transmission lines and could be capacitive or inductive depending on the matching approach; it will however be considered to be capacitive for the purposes of the analysis.

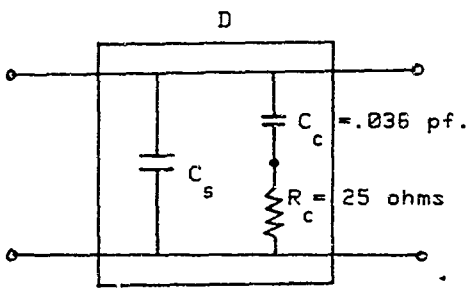


Figure B-3. Shunt Tap Network D

An analysis of the tap voltages was performed using equations (B-8) and (B-9) and the shunt tap network of Figure B-3. For this analysis, the following parameters were used:

Dielectric Constant of TL	= 2.2
Tap Spacing of D	= 1.1 inches
Coupling Capacitance, C_C	= 0.36 picofarad
Shunt Capacitance, C_S	= Variable
Number of taps, n	= Variable
Reflection Coefficients at loop ends, R_L and R_R	= Variable

Figures B-4 through B-7 show the total rms errors (amplitude and phase) of the tap output V^i relative to the average amplitude and phase for n ports with perfect loads (no reflections, $R_R = R_L = 0$) on the loop ends. Two cases are shown, an even number of taps (32) and an odd number of taps (330 for several different values of shunt capacitance. The results indicate that the total error can be quite large if the taps are not matched and when the spacing between taps is a multiple of a half wavelength in the transmission line. For the 1.1 inch tap spacing, which is approximately 0.5 wavelengths at 5.4 GHz in free space, the taps are spaced at 0.5 wavelength at 3.6 GHz and 1 wave length at 7.2 GHz in the transmission line. The operating frequency for the calibrator is 5.2 to 5.7 GHz which puts the tap spacing approximately 0.75 wave lengths apart (at 5.4 GHz) over the frequency range. The even number of taps is seen to have a lower error than an odd number of taps for a nominal tap spacing of 0.75 wave lengths along the transmission line. The worst case mismatch of $C_S = 6$ picofarads corresponds to a VSWR of 1.2 for a single tap network at 5.4 GHz.

Figures B-8 and B-9 show the total rms error levels when the shunt reflection is matched ($C_S = 0$) but their are load mismatches on the ends of the loop. As in the previous cases, an odd number of taps has somewhat larger errors than an even number of taps for the 0.75 wave length tap spacings. Further it is necessary to suppress both the shunt and load end mismatches to reduce the error contribution from the loop calibrator network.

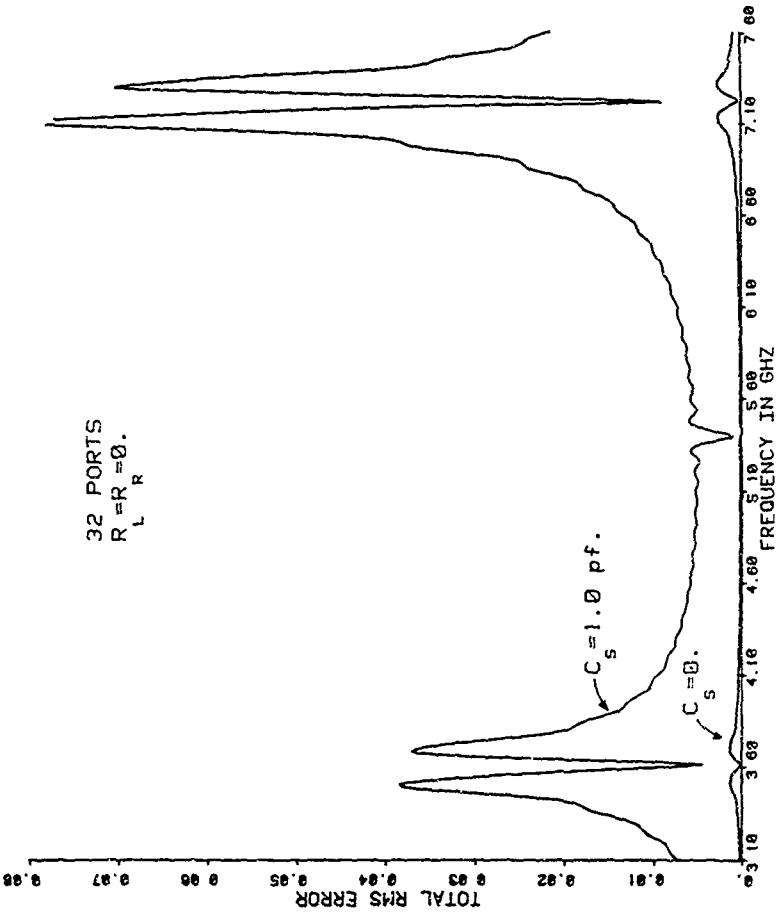


Figure B-4. 32 Port Calibration Feed With Shunt Mismatches

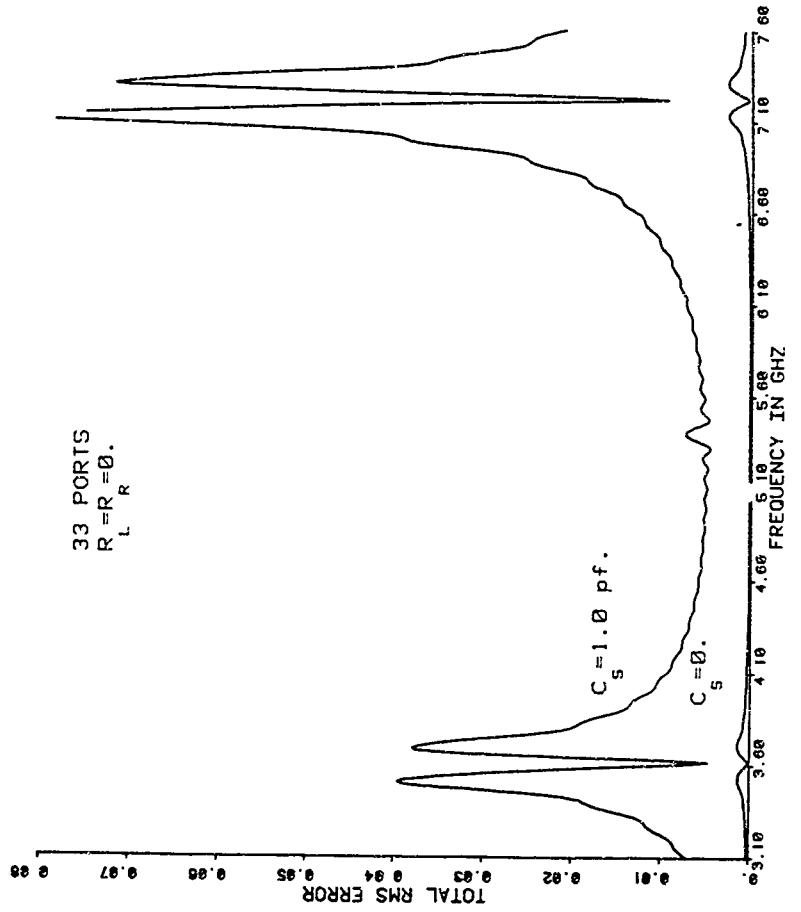


Figure B-5. 33 Port Calibration Feed With Shunt Mismatches

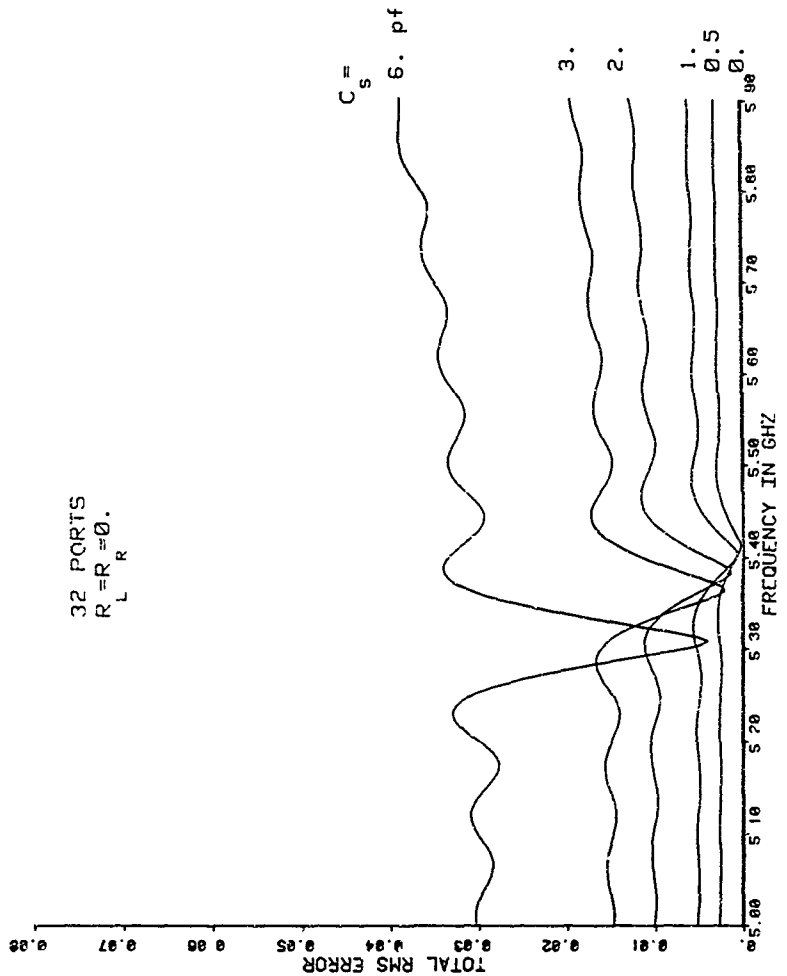


Figure B-6. 32 Port Calibration Feed With Shunt Mismatches

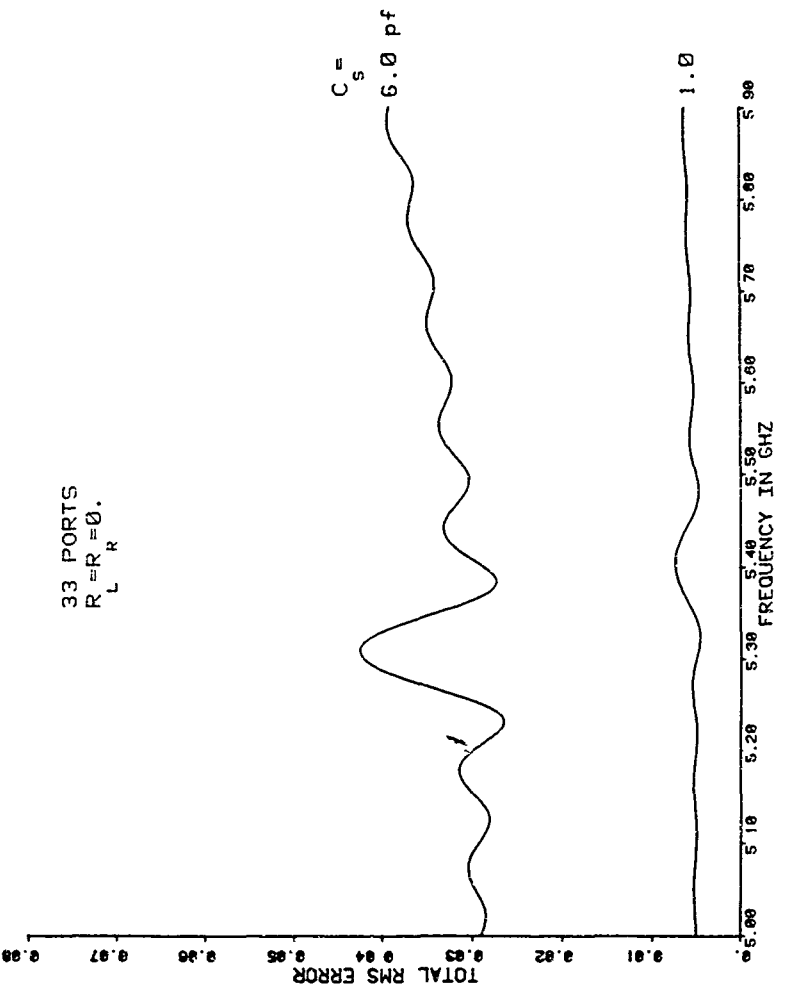


Figure B-7. 33 Port Calibration Feed With Shunt Mismatches

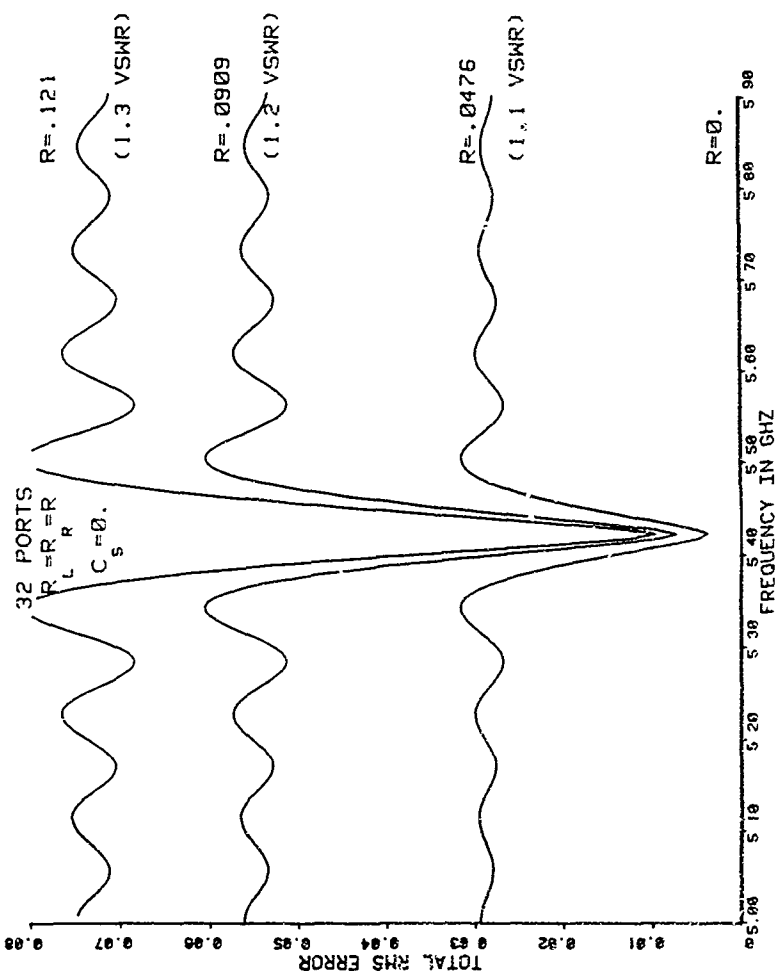


Figure B-8. 32 Port Calibration Feed With Load Mismatches

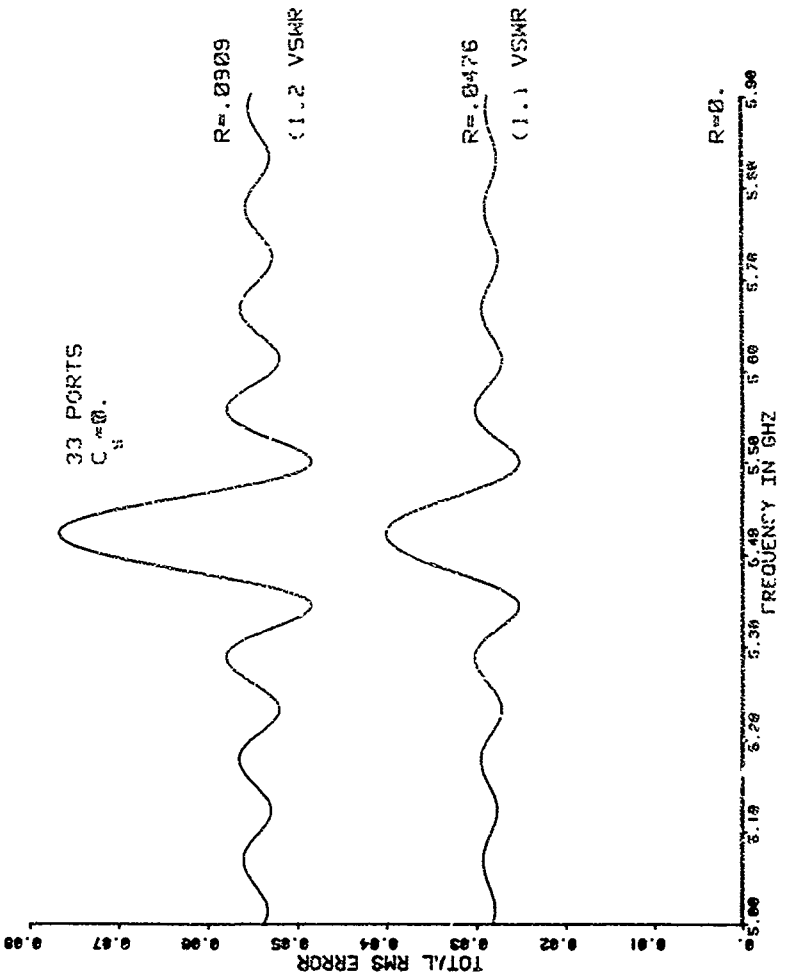


Figure B-9. 33 Port Calibration Feed With Load Mismatches

The distribution of the amplitude and phase errors for a 32 port loop calibrator with mismatched taps and perfectly matched end loads are shown in Figures B-10 and B-11 which correspond to operating frequencies of 5.2 and 5.7 GHz (edge of band frequencies). The errors are seen to be highly correlated with a periodicity corresponding to two port spacings on the calibrator feed. Similar results are obtained when the shunt admittance of the taps is matched but the end loads are mismatched.

The impact of the calibrator errors on the array factor patterns is illustrated in Figures B-12 through B-15 for a 32 element line array spaced at 1.1 inches with 40 dB, nbar 6 Taylor weights. Figure B-12 illustrates the array factor pattern with no errors. Figures B-13 and B-14 show superimposed array factor patterns from 5.2 to 5.7 GHz with only one source of mismatch error (shunt taps and load end mismatches respectively) present at a time. The last Figure B-15, shows the array pattern at 5.2 GHz with a composite shunt tap and load mismatches. The highly correlated errors in the loop calibrator produce peaks in the sidelobes which are spaced far from the main beam; the peak sidelobe levels correspond to the total rms errors.

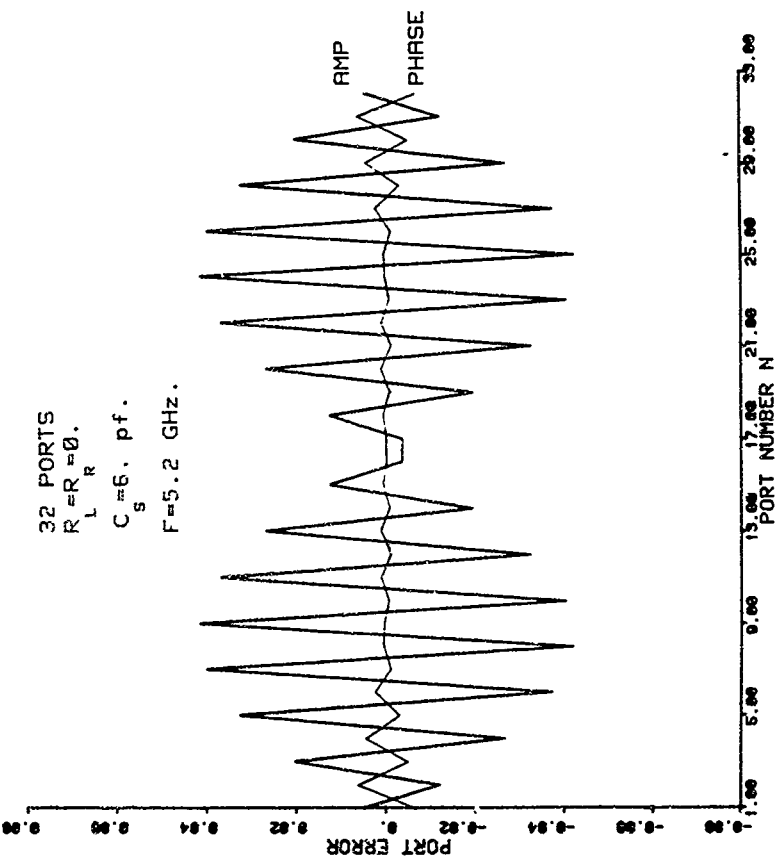


Figure B-10. Errors At Tap Outputs Of 32 Port Feed Witn Shunt Mismatches

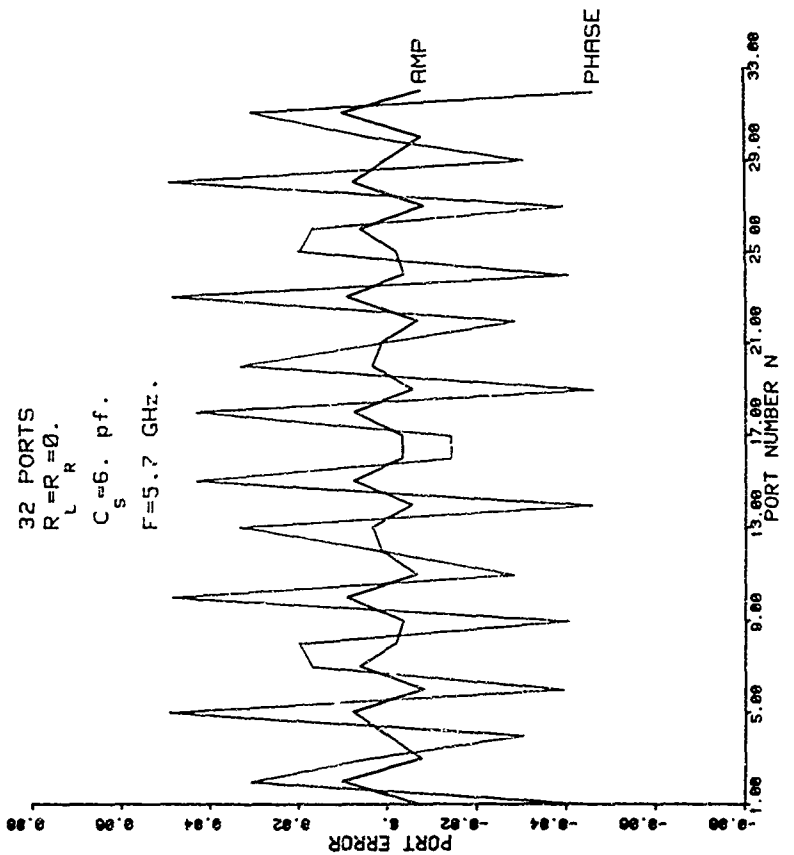


Figure B-11. Errors At Tap Outputs Of 32 Port Feed With Shunt and Load Mismatches

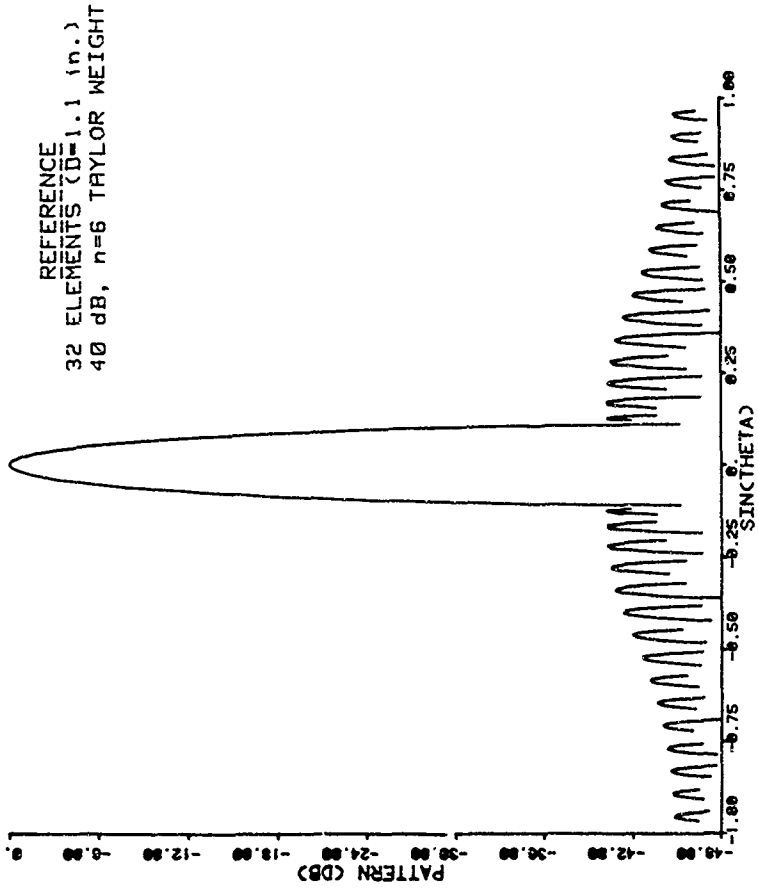


Figure B-12. Ideal Array Factor Patterns

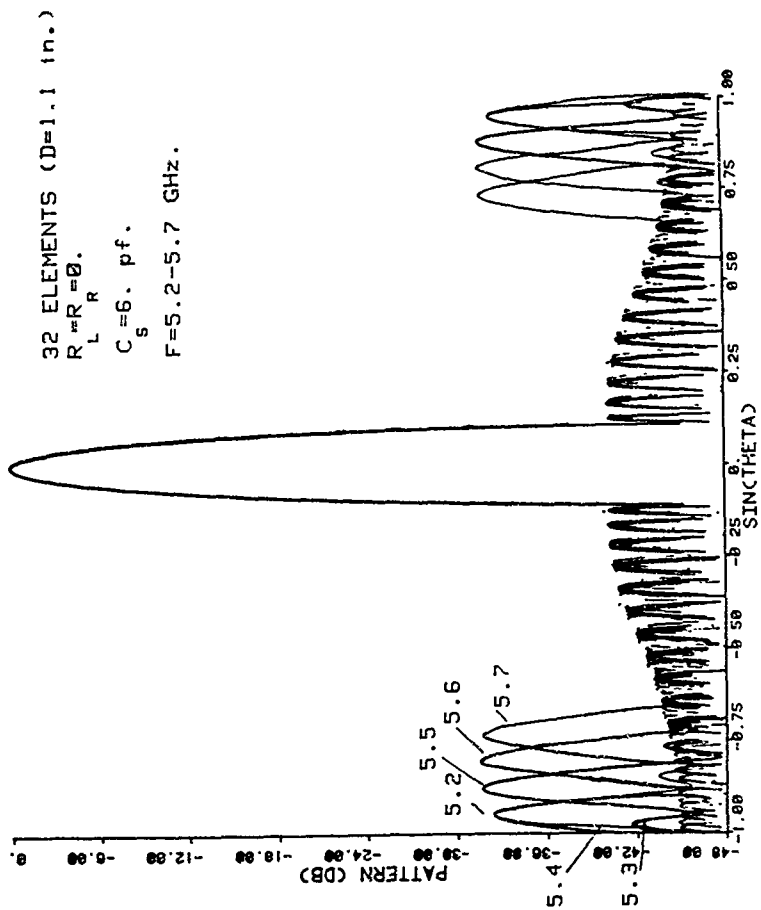


Figure B-13. Array Factor Pattern With Shunt Mismatches

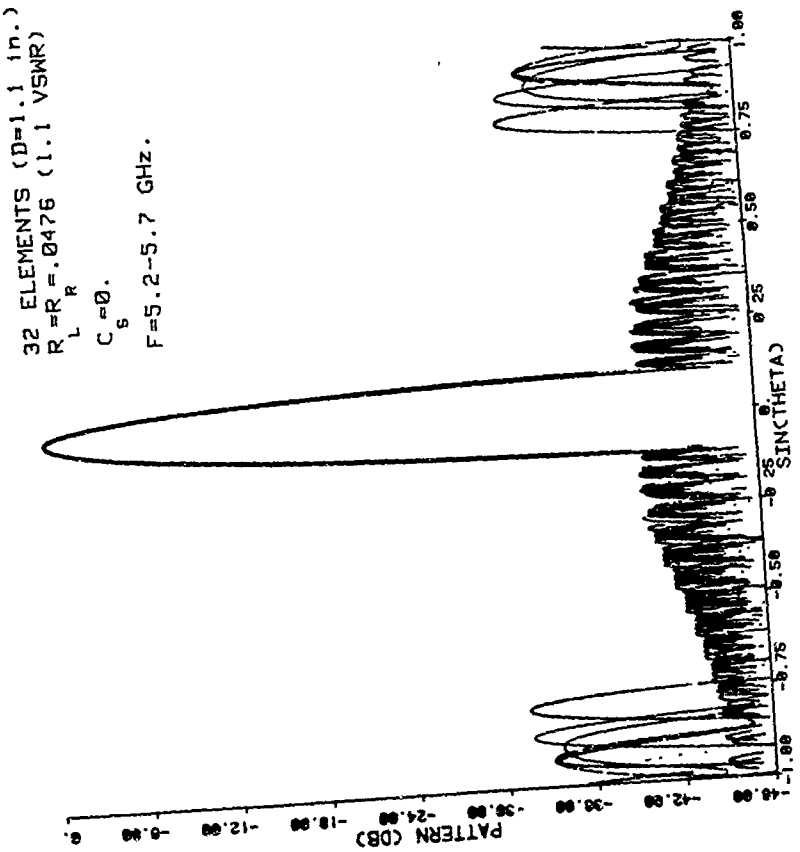


Figure B-14. Array Factor Pattern With Load Mismatches

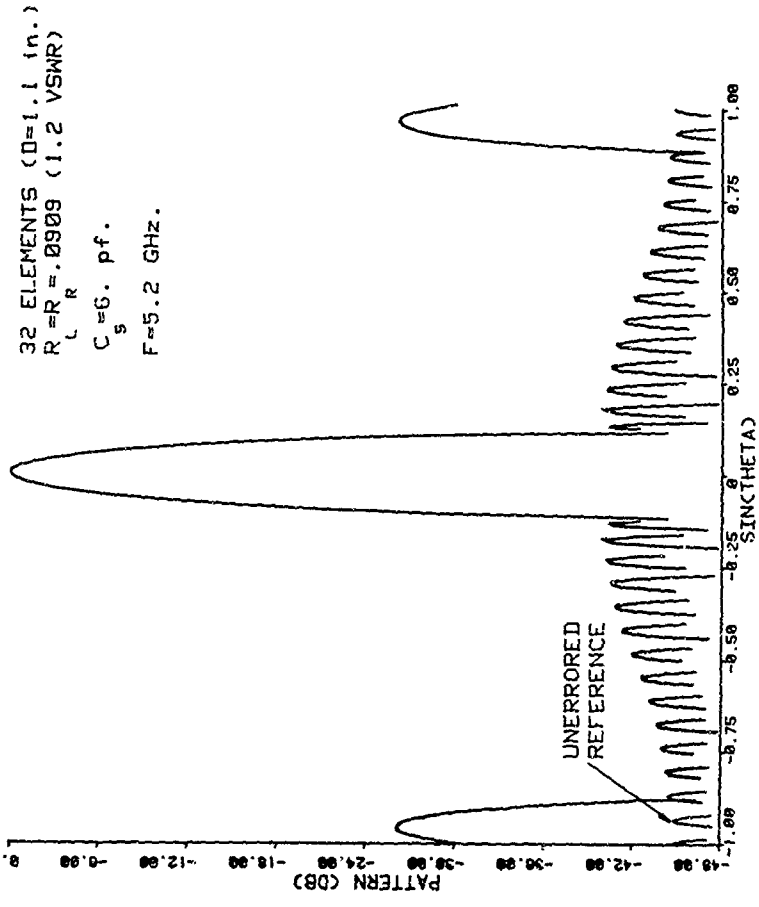


Figure B-15. Array Factor Pattern With Combined Mismatches

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